

**Figure 3 HS400 reference load**

**HS400 Capacitance**

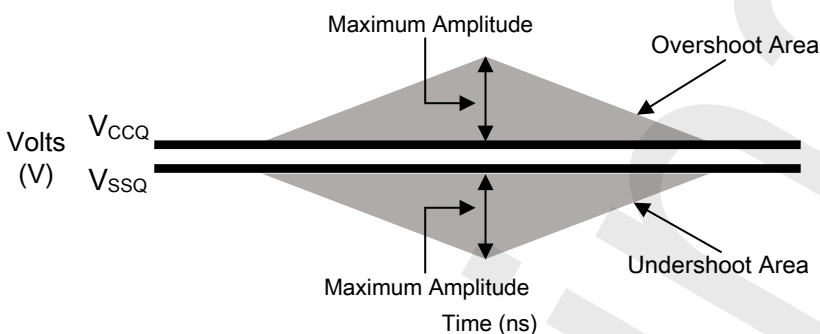
The Data Strobe is used to read data in HS400 mode. The Data Strobe is toggled only during data read or CRC status response.

Parameter	Symbol	Min	Typ.	Max	Unit	Remark
Pull-up resistance for CMD	R <sub>CMD</sub>	4.7		100 <sup>Note 1</sup>	kΩ	
Pull-up resistance for DAT0-7	R <sub>DAT</sub>	10		100 <sup>Note 1</sup>	kΩ	
Pull-down resistance for Data Strobe	R <sub>DS</sub>	10		100 <sup>Note 1</sup>	kΩ	
Internal pull up resistance DAT1-DAT7	R <sub>int</sub>	10		150	kΩ	
Single Device capacitance	C <sub>DEVICE</sub>			6	pF	

Note 1: Recommended maximum value is 50 kΩ for 1.8 V interface supply voltages.

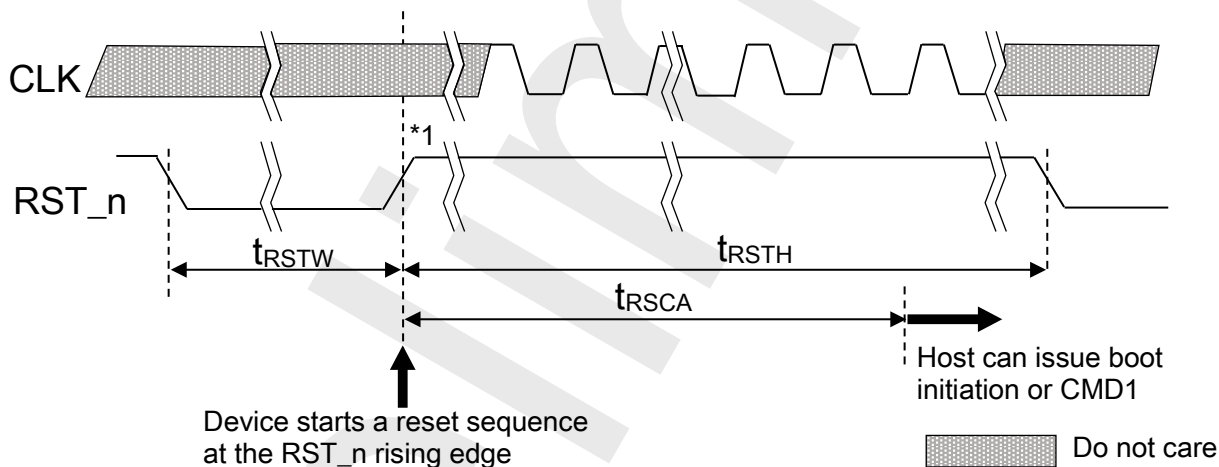
**Overshoot/Undershoot Specification**

		V <sub>CCQ</sub>	Unit
		1.70V - 1.95V	
Maximum peak amplitude allowed for overshoot area. (See Figure Overshoot/Undershoot definition)	Max	0.9	V
Maximum peak amplitude allowed for undershoot area. (See Figure Overshoot/Undershoot definition)	Max	0.9	V
Maximum area above V <sub>CCQ</sub> (See Figure Overshoot/Undershoot definition)	Max	1.5	V-ns
Maximum area below V <sub>SSQ</sub> (See Figure Overshoot/Undershoot definition)	Max	1.5	V-ns



**Figure 4 Overshoot/Undershoot definition**

**H/W Reset Operation**



\*1: Device will detect the rising edge of RST\_n signal to trigger internal reset sequence.

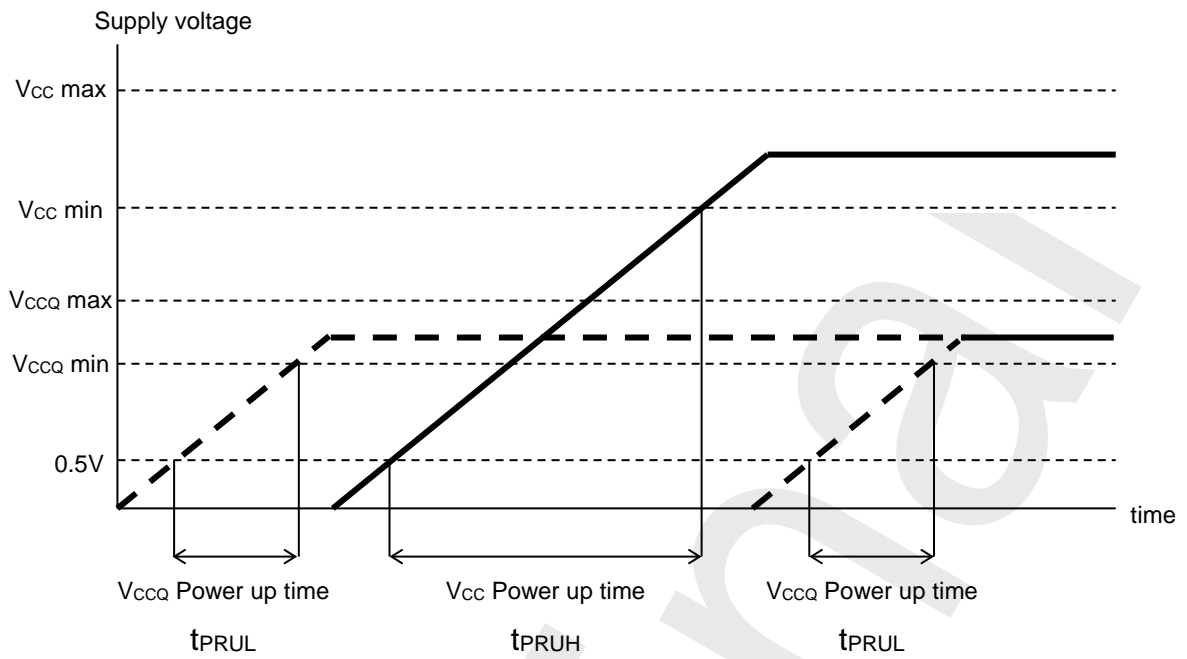
**H/W Reset Timings**

Symbol	Parameter	Min	Max	Unit
t <sub>RSTW</sub>	RST_n pulse width	1	—	μs
t <sub>RSCA</sub>	RST_n to Command time	200 <sup>Note 1</sup>	—	μs
t <sub>RSTH</sub>	RST_n high period (interval time)	1	—	μs

Note 1: 74 cycles of clock signal required before issuing CMD1 or CMD0 with argument 0xFFFFFFFF.

Note 2: During the device internal initialization sequence right after power on, device may not be able to detect RST\_n signal, because the device may not complete loading RST\_n\_ENABLE bits of the extended CSD register into the controller yet.

**Power-up sequence**



**Figure 5 Power up sequence**

**Power-up parameter**

Parameter	Symbol	Min	Max	Remark
Supply power-up for 3.3V	t <sub>PRUH</sub>	5 μs	35 ms	-
Supply power-up for 1.8V	t <sub>PRUL</sub>	5 μs	25 ms	-

**Functional restrictions**

- Pre loading data size is limited to MAX\_PRE\_LOADING\_DATA\_SIZE[21-18] regardless of using Production State Awareness function.
- MAX\_PRE\_LOADING\_DATA\_SIZE[21-18] value will change when host sets Enhanced User area Partition.

**Reliability Guidance**

This reliability guidance is intended to notify some guidance related to using raw NAND flash. Although random bit errors may occur during use, it does not necessarily mean that a block is bad. Generally, a block should be marked as bad when a program status failure or erase status failure is detected. The other failure modes may be recovered by a block erase. ECC treatment for read data is mandatory due to the following Data Retention and Read Disturb failures.

**-Write/Erase Endurance**

Write/Erase endurance failures may occur in a cell, page, or block, and are detected by doing a status read after either an auto program or auto block erase operation. The cumulative bad block count will increase along with the number of write/erase cycles.

**-Data Retention**

The data in memory may change after a certain amount of storage time. This is due to charge loss or charge gain. After block erasure and reprogramming, the block may become usable again. Also write/erase endurance deteriorates data retention capability. The figure below shows a generic trend of relationship between write/erase endurance and data retention.

**-Read Disturb**

A read operation may disturb the data in memory. The data may change due to charge gain. Usually, bit errors occur on other pages in the block, not the page being read. After a large number of read cycles (between block erases), a tiny charge may build up and can cause a cell to be soft programmed to another state. After block erasure and reprogramming, the block may become usable again.

Considering the above failure modes, Toshiba Memory recommends following usage:

- Please avoid any excessive iteration of resets and initialization sequences (Device identification mode) as far as possible after power-on, which may result in read disturb failure. The resets include hardware resets and software resets.

e.g.1) Iteration of the following command sequence, CMD0 - CMD1 ---

The assertion of CMD1 implies a count of internal read operation in Raw NAND.

CMD0: Reset command, CMD1: Send operation command

e.g.2) Iteration of the following commands, CMD30 and/or CMD31

CMD30: Send status of write protection bits, CMD31: Send type of write protection

**Document Revision History**

Rev.0.1      January 31st, 2019      - Released as preliminary revision

preliminary

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