PMS150C
8bit OTP Type IO Controller

Data Sheet

Version 0.04 – Jan. 24, 2018
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PMS150C is NOT designed for AC RC step-down powered, high power ripple or high EFT requirement application, please do NOT apply PMS150C to those application products.
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<th>Date</th>
<th>Description</th>
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<tr>
<td></td>
<td></td>
<td>1st version</td>
</tr>
<tr>
<td>0.01</td>
<td>2016/03/09</td>
<td>1. Amend Chapter 2 Block Diagram&lt;br&gt;2. Amend Chapter 4.1 Pull-high Resistance typical value&lt;br&gt;3. Add Chapter 5.5 and all descriptions about the Comparator&lt;br&gt;4. Add Chapter 5.7 and all descriptions about Timer2 with PWM generation</td>
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<tr>
<td>0.02</td>
<td>2016/11/03</td>
<td>1. Amend Section 1.1 System Features&lt;br&gt;2. Add Section 1.3 Package Information&lt;br&gt;3. Amend Chapter 3 Pin Functional Description: PMS150C-U06, PMS150C-S08, PMS150C-D08&lt;br&gt;4. Amend Section 4.1 DC/AC Characteristics: “VIL” and “VIH”&lt;br&gt;5. Amend Section 4.11 Typical IO input high/low threshold voltage&lt;br&gt;6. Add Section 4.12. Typical power down current (IpD) and power save current (IpS)&lt;br&gt;7. Add Section 5.2.1 Timing charts for reset conditions&lt;br&gt;8. Amend Section 5.4 Oscillator and clock&lt;br&gt;9. Amend Section 5.4.3 IHRC Frequency Calibration and System Clock&lt;br&gt;10. Amend Section 5.4.4 System Clock and LVR levels&lt;br&gt;11. Amend Fig.2 Options of System Clock&lt;br&gt;12. Amend Section 5.5.2 description about the comparator Case A and Case B&lt;br&gt;13. Amend Section 5.6 16-bit Timer&lt;br&gt;14. Amend Section 5.8 Watchdog Timer&lt;br&gt;15. Amend Section 5.9 Interrupt&lt;br&gt;16. Amend Fig.12 Hardware diagram of Interrupt controller&lt;br&gt;17. Amend Section 5.10.1 Power-Save mode&lt;br&gt;18. Amend Section 5.10.3 Wake-up&lt;br&gt;19. Amend Section 6.3 Clock Mode Register&lt;br&gt;20. Amend Section 6.13 MISC Register&lt;br&gt;21. Amend Section 6.14. Comparator Control Register&lt;br&gt;22. Amend Section 6.16. Timer2 Control Register&lt;br&gt;23. Delete the Symbol “pc0” in Chapter 7&lt;br&gt;24. Add Chapter 8 Code Options&lt;br&gt;25. Amend Section 9.2.1 IO pin usage and setting&lt;br&gt;26. Amend Section 9.2.4 Power down mode, wakeup and watchdog&lt;br&gt;27. Add Section 9.2.6 IHRC&lt;br&gt;28. Amend Section 9.2.7 LVR&lt;br&gt;29. Amend Section 9.2.10 Program writing&lt;br&gt;30. Amend Section 9.3 Using ICE</td>
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<tr>
<td>0.03</td>
<td>2017/12/04</td>
<td>1. Amend the address and phone number of PADAUK Technology Co.,Ltd.&lt;br&gt;2. Amend Section 1.2 CPU Features&lt;br&gt;3. Amend Section 5.4.4 System Clock and LVR levels&lt;br&gt;4. Amend Section 5.5.2 Using the comparator&lt;br&gt;5. Amend Section 5.5.3 Using the comparator and band-gap 1.20V&lt;br&gt;6. Amend Section 5.9 Interrupt&lt;br&gt;7. Amend Section 5.10.1 Power-Save mode&lt;br&gt;8. Amend Section 5.10.2 Power-Down mode&lt;br&gt;9. Amend Section 5.10.3 Wake-up&lt;br&gt;10. Amend Section 6.15 Comparator Selection Register (gpcs)</td>
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# Major Differences between PMS150B and PMS150C

<table>
<thead>
<tr>
<th>Item</th>
<th>Function</th>
<th>PMS150B</th>
<th>PMS150C</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Frequency of ILRC</td>
<td>110KHz@5V, 25 °C (much smaller variant with VDD changes)</td>
<td>62KHz@5V, 25 °C (much smaller variant with VDD changes)</td>
</tr>
<tr>
<td>2</td>
<td>LVR levels</td>
<td>2.8V, 2.2V, 2.0V</td>
<td>4.0V, 3.5V, 3.0V, 2.75V, 2.5V, 2.2V, 2.0V, 1.8V</td>
</tr>
<tr>
<td>3</td>
<td>Data RAM</td>
<td>60 bytes</td>
<td>64 bytes</td>
</tr>
<tr>
<td>4</td>
<td>Input pull-up resistor of PA5</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>5</td>
<td>Operation temperature</td>
<td>0 °C ~70 °C</td>
<td>-20 °C ~70 °C</td>
</tr>
<tr>
<td>6</td>
<td>Power save current (stoplex)</td>
<td>40μ<a href="mailto:A@3.3V">A@3.3V</a></td>
<td>3μA @3.3V</td>
</tr>
<tr>
<td>7</td>
<td>IO Sink / Drive current</td>
<td>17mA / -7mA@5V</td>
<td>Normal: 14.5mA / -10.5mA@5V Low: 5mA / -3.5mA@5V</td>
</tr>
<tr>
<td>8</td>
<td>Watchdog timeout period</td>
<td>4096, 16384, 65536 T&lt;sub&gt;ILRC&lt;/sub&gt;</td>
<td>8k, 16k, 64k, 256k T&lt;sub&gt;ILRC&lt;/sub&gt;</td>
</tr>
<tr>
<td>9</td>
<td>Wake-up time (t&lt;sub&gt;WUP&lt;/sub&gt;)</td>
<td>Fast: 1024 T&lt;sub&gt;ihrc&lt;/sub&gt; Slow: 1024 T&lt;sub&gt;ilrc&lt;/sub&gt;</td>
<td>Fast: 32 T&lt;sub&gt;ilrc&lt;/sub&gt; Slow: 2048 T&lt;sub&gt;ilrc&lt;/sub&gt;</td>
</tr>
<tr>
<td>10</td>
<td>Boot-up time</td>
<td>Fast: 2048 T&lt;sub&gt;ihrc&lt;/sub&gt; Slow: 1024 T&lt;sub&gt;ilrc&lt;/sub&gt;</td>
<td>Fast: 32 T&lt;sub&gt;ilrc&lt;/sub&gt; Slow: 2048 T&lt;sub&gt;ilrc&lt;/sub&gt;</td>
</tr>
<tr>
<td>11</td>
<td>System reserved OTP area</td>
<td>0x3F8 ~ 0x3FF (8 words)</td>
<td>0x3F0 ~ 0x3FF (16 words)</td>
</tr>
<tr>
<td>12</td>
<td>ILRC modes for system CLK</td>
<td>ILRC, ILRC/4</td>
<td>ILRC, ILRC/4, ILRC/16</td>
</tr>
<tr>
<td>13</td>
<td>Supporting ICE</td>
<td>PDK3S-I-00x (recommended not to use) 5S-I-S0xx</td>
<td>5S-I-S0xx</td>
</tr>
<tr>
<td>14</td>
<td>8-bit Timer2 with PWM</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>15</td>
<td>Comparator</td>
<td>No</td>
<td>Yes</td>
</tr>
</tbody>
</table>
1. Features

1.1. System Features
- 1KW OTP program memory
- 64 Bytes data RAM
- One hardware 16-bit timer
- One hardware 8-bit timer with PWM generation
- One general purpose comparator
- Support fast wake-up
- Every IO pin can be configured to enable wake-up function
- 6 IO pins with optional drive/sink current and pull-high resistor
- Clock sources: internal high RC oscillator and internal low RC oscillator
- Eight levels of LVR ~ 4.0V, 3.5V, 3.0V, 2.75V, 2.5V, 2.2V, 2.0V, 1.8V
- One external interrupt pin

1.2. CPU Features
- One processing unit operating mode
- 79 Powerful instructions
- Most instructions are 1T execution cycle
- Programmable stack pointer and adjustable stack level
- All data memories are available for use as an index pointer
- IO space and memory space are independent

1.3. Package Information
- PMS150C Series
  - PMS150C - U06: SOT23-6 (60mil);
  - PMS150C - S08: SOP8 (150mil);
  - PMS150C - D08: DIP8 (300mil)
2. General Description and Block Diagram

The PMS150C is an IO-Type, fully static, OTP-based controller; it employs RISC architecture and most the instructions are executed in one cycle except that few instructions are two cycles that handle indirect memory access. 1KW bits OTP program memory and 64 bytes data SRAM are inside. Besides, one hardware 16-bit timer, one hardware 8-bit timer with PWM generation and one general purpose comparator are also provided in the PMS150C.
3. Pin Functional Description

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin &amp; Buffer Type</th>
<th>Description</th>
</tr>
</thead>
</table>
| PA7 / CIN3- | IO ST / CMOS / Analog | This pin can be used as:  
(1) Bit 7 of port A. It can be configured as digital input, two-state output with pull-up resistor by software independently.  
(2) Minus input source 3 of comparator. When this pin is configured as analog input, please use bit 7 of register padier to disable the digital input to prevent current leakage. This pin can be used to wake-up system during sleep mode; however, wake-up function is also disabled if bit 7 of padier register is “0”. |
| PA6 / CIN2- | IO ST / CMOS / Analog | This pin can be used as:  
(1) Bit 6 of port A. It can be configured as digital input, two-state output with pull-up resistor by software independently.  
(2) Minus input source 2 of comparator. When this pin is configured as analog input, please use bit 6 of register padier to disable the digital input to prevent current leakage. This pin can be used to wake-up system during sleep mode; however, wake-up function is also disabled if bit 6 of padier register is “0”. |
<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin &amp; Buffer Type</th>
<th>Description</th>
</tr>
</thead>
</table>
| PA5 / PRST# | IO ST / CMOS | The functions of this pin can be:  
(1) Bit 5 of port A. It can be configured as input or open-drain output pin with pull-up resistor.  
(2) Hardware reset.  
This pin can be used to wake-up system during sleep mode; however, wake-up function is also disabled if bit 5 of `padier` register is “0”.  
Please put 33Ω resistor in series to have high noise immunity when this pin is in input mode. |
| PA4 / CIN+/ CIN4-/ TM2PWM | IO ST / CMOS / Analog | This pin can be used as:  
(1) Bit 4 of port A. It can be configured as digital input, two-state output with pull-up resistor by software independently.  
(2) Plus input source of comparator.  
(3) Minus input source 4 of comparator.  
(4) Output of 8-bit Timer2 (TM2)  
When this pin is configured as analog input, please use bit 4 of register `padier` to disable the digital input to prevent current leakage. This pin can be used to wake-up system during sleep mode; however, wake-up function is also disabled if bit 4 of `padier` register is “0”. |
| PA3 / CIN1-/ TM2PWM | IO ST / CMOS / Analog | This pin can be used as:  
(1) Bit 3 of port A. It can be configured as digital input, two-state output with pull-up resistor by software independently.  
(2) Minus input source 1 of comparator.  
(3) Output of 8-bit Timer2 (TM2)  
When this pin is configured as analog input, please use bit 3 of register `padier` to disable the digital input to prevent current leakage. This pin can be used to wake-up system during sleep mode; however, wake-up function is also disabled if bit 3 of `padier` register is “0”. |
| PA0 / INT0 / CO | IO ST / CMOS | The functions of this pin can be:  
(1) Bit 0 of port A. It can be configured as input or output with pull-up resistor.  
(2) External interrupt line 0. Both rising edge and falling edge are accepted to request interrupt service.  
(3) Output of comparator  
This pin can be used to wake up system during sleep mode; however, wake-up function from this pin is also disabled when bit 0 of `padier` register is “0”. |
| VDD | Positive power | |
| GND | Ground | |

Notes: IO: Input/Output; ST: Schmitt Trigger input; Analog: Analog input pin; CMOS: CMOS voltage level
4. Device Characteristics

4.1. DC/AC Characteristics

All data are acquired under the conditions of \( V_{DD} = 5.0V, f_{SYS} = 2MHz \) unless noted.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{DD} )</td>
<td>Operating Voltage</td>
<td>2.0*</td>
<td>5.5</td>
<td>V</td>
<td>* Subject to LVR tolerance</td>
<td></td>
</tr>
<tr>
<td>LVR%</td>
<td>Low Voltage Reset tolerance</td>
<td>-5</td>
<td>5</td>
<td>%</td>
<td>( V_{DD} \leq 3.0V )</td>
<td></td>
</tr>
<tr>
<td>( f_{SYS} )</td>
<td>System clock (CLK)* = ( \frac{IHRC}{2} )</td>
<td>0</td>
<td>8M</td>
<td>Hz</td>
<td>( V_{DD} \geq 3.0V )</td>
<td></td>
</tr>
<tr>
<td></td>
<td>( \frac{IHRC}{4} )</td>
<td>0</td>
<td>4M</td>
<td>Hz</td>
<td>( V_{DD} \geq 2.2V )</td>
<td></td>
</tr>
<tr>
<td></td>
<td>( \frac{IHRC}{8} )</td>
<td>0</td>
<td>2M</td>
<td>Hz</td>
<td>( V_{DD} \geq 2.0V )</td>
<td></td>
</tr>
<tr>
<td></td>
<td>ILRC</td>
<td>62K</td>
<td></td>
<td></td>
<td>( V_{DD} = 5.0V )</td>
<td></td>
</tr>
<tr>
<td>( V_{POR} )</td>
<td>Power On Reset Voltage</td>
<td>1.9</td>
<td>2.0</td>
<td>2.1</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( I_{OP} )</td>
<td>Operating Current</td>
<td>0.3/13</td>
<td>mA/uA</td>
<td>f(_{SYS}) = IHRC/16 = <a href="mailto:1MIPS@3.3V">1MIPS@3.3V</a></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{PD} )</td>
<td>Power Down Current (by ( \text{stopsys} ) command)</td>
<td>0.5</td>
<td>uA</td>
<td>f(<em>{SYS}) = 0Hz, ( V</em>{DD} = 3.3V )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{PS} )</td>
<td>Power Save Current (by ( \text{stopexe} ) command)</td>
<td>3</td>
<td>uA</td>
<td>( V_{DD} = 3.3V ); Band-gap, LVR, IHRC are OFF, ILRC module is ON.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{IL} )</td>
<td>Input low voltage for IO lines</td>
<td>0</td>
<td>0.1 ( V_{DD} )</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{IH} )</td>
<td>Input high voltage for IO lines</td>
<td>0.8 ( V_{DD} )</td>
<td>( V_{DD} )</td>
<td>V</td>
<td>PA5 Others IO</td>
<td></td>
</tr>
<tr>
<td>( I_{OL} )</td>
<td>IO lines sink current Normal</td>
<td>10/3.5</td>
<td>14.5/5.0</td>
<td>19/6.5</td>
<td>mA</td>
<td>( V_{DD} = 5.0V, V_{OL} = 0.5V )</td>
</tr>
<tr>
<td></td>
<td>Low</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{OH} )</td>
<td>IO lines drive current Normal</td>
<td>-7.5/-2.6</td>
<td>-10.5/-3.5</td>
<td>-13.5/-4.4</td>
<td>mA</td>
<td>( V_{DD} = 5.0V, V_{OH} = 4.5V )</td>
</tr>
<tr>
<td></td>
<td>Low</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{IN} )</td>
<td>Input voltage</td>
<td>-0.3</td>
<td>( V_{DD} + 0.3 )</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{INJ(PIN)} )</td>
<td>Injected current on pin</td>
<td>1</td>
<td>mA</td>
<td>( V_{DD} + 0.3 \geq V_{IN} \geq -0.3 )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( R_{PH} )</td>
<td>Pull-high Resistance</td>
<td>100/220</td>
<td>KΩ</td>
<td>( V_{DD} = 5.0V )</td>
<td>( V_{DD} = 3.3V )</td>
<td></td>
</tr>
<tr>
<td>( f_{IHRC} )</td>
<td>Frequency of IHRC after calibration*</td>
<td>15.76/15.20</td>
<td>16*/16*</td>
<td>16.24*/16.80*</td>
<td>MHz</td>
<td>( V_{DD} = 2.0V \pm 5.5V, )</td>
</tr>
<tr>
<td></td>
<td></td>
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<td></td>
<td></td>
<td>(-20^\circ C &lt; Ta &lt; 70^\circ C)</td>
<td></td>
</tr>
<tr>
<td>( f_{ILRC} )</td>
<td>Frequency of ILRC*</td>
<td>62*</td>
<td>KHz</td>
<td>( V_{DD} = 5.0V, -20^\circ C &lt; Ta &lt; 70^\circ C )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{INT} )</td>
<td>Interrupt pulse width</td>
<td>30</td>
<td>ns</td>
<td>( V_{DD} = 5.0V )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{DR} )</td>
<td>RAM data retention voltage*</td>
<td>1.5</td>
<td>V</td>
<td>In power-down mode.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{WDT} )</td>
<td>Watchdog timeout period</td>
<td>8k/16/64/256</td>
<td>ILRC clock period</td>
<td>( \text{misc}[1:0] = (00, 01, 10, 11) )</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### 4.2. Absolute Maximum Ratings

- **Supply Voltage** ........................................... 2.0V ~ 5.5V (Maximum Rating: 5.5V)
  
  *If VDD over maximum rating, it may lead to a permanent damage of IC.

- **Input Voltage** ........................................... -0.3V ~ VDD + 0.3V

- **Operating Temperature** .............................. -20°C ~ 70°C

- **Storage Temperature** ................................. -50°C ~ 125°C

- **Junction Temperature** ................................. 150°C
4.3. Typical IHRC Frequency vs. VDD (calibrated to 16MHz)

![IHRC Frequency vs. VDD](image)

4.4. Typical ILRC Frequency vs. VDD

![ILRC Frequency Deviation vs. VDD](image)
4.5. Typical IHRC Frequency vs. Temperature (calibrated to 16MHz)

![IHRC Drift Graph]

4.6. Typical ILRC Frequency vs. Temperature

![ILRC Drift Graph]
4.7. Typical Operating Current vs. VDD and CLK=IHRC/n

Conditions: **ON**: Band-gap, LVR, IHRC, T16 modules; **OFF**: ILRC modules;
**IO**: PA0: 0.5Hz output toggle and no loading, others: input and no floating

![IHRC/n vs. VDD](image)

4.8. Typical Operating Current vs. VDD and CLK=ILRC/n

Conditions: **ON**: T16 modules; **OFF**: Band-gap, LVR, ILRC, IHRC modules;
**IO**: PA0: 0.5Hz output toggle and no loading, others: input and no floating

![ILRC/n vs. VDD](image)
4.9. Typical IO pull high resistance

![Pull High Resistor Graph]

4.10. Typical IO driving current (IoH) and sink current (IoL)

![Avg. IoH, IoL vs. VDD Graph]
4.11. Typical IO input high/low threshold voltage ($V_{IH}/V_{IL}$)

\[ \begin{array}{c|c|c|c}
V_{DD} (V) & V_{IH} (V) & V_{IL} (V) \\
\hline
2.0 & 2.0 & 0.0 \\
2.5 & 2.5 & 0.5 \\
3.0 & 3.0 & 1.0 \\
3.5 & 3.5 & 1.5 \\
4.0 & 4.0 & 2.0 \\
4.5 & 4.5 & 2.5 \\
5.0 & 5.0 & 3.0 \\
5.5 & 5.5 & 3.5 \\
\end{array} \]
4.12. Typical power down current ($I_{PD}$) and power save current ($I_{PS}$)

**stopsys power down current vs. VDD**

![Graph showing stopsys power down current vs. VDD.](image1)

**stopexe power save current vs. VDD**

![Graph showing stopexe power save current vs. VDD.](image2)
5. Functional Description

5.1. Program Memory – OTP

The OTP (One Time Programmable) program memory is used to store the program instructions to be executed. The OTP program memory may contain the data, tables and interrupt entry. After reset, the initial address for FPP0 is 0x000. The interrupt entry is 0x010 if used, the last 16 addresses are reserved for system using, like checksum, serial number, etc. The OTP program memory for PMS150C is 1KW that is partitioned as Table 1. The OTP memory from address 0x3F0 to 0x3FF is for system using, address space from 0x001 to 0x00F and from 0x011 to 0x3EF is user program space.

<table>
<thead>
<tr>
<th>Address</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x000</td>
<td>FPP0 reset – goto instruction</td>
</tr>
<tr>
<td>0x001</td>
<td>User program</td>
</tr>
<tr>
<td>...</td>
<td></td>
</tr>
<tr>
<td>0x00F</td>
<td>User program</td>
</tr>
<tr>
<td>0x010</td>
<td>Interrupt entry address</td>
</tr>
<tr>
<td>0x011</td>
<td>User program</td>
</tr>
<tr>
<td>...</td>
<td></td>
</tr>
<tr>
<td>0x3EF</td>
<td>User program</td>
</tr>
<tr>
<td>0x3F0</td>
<td>System Using</td>
</tr>
<tr>
<td>...</td>
<td></td>
</tr>
<tr>
<td>0x3FF</td>
<td>System Using</td>
</tr>
</tbody>
</table>

Table 1: Program Memory Organization

5.2. Boot Procedure

POR (Power-On-Reset) is used to reset PMS150C when power up, the boot up time can be optional fast or slow, time for fast boot-up is about 32 ILRC clock cycles and 2048 ILRC clock cycles for slow boot-up. Customer must ensure the stability of supply voltage after power up no matter which option is chosen, the power up sequence is shown in the Fig. 1 and \( t_{SBP} \) is the boot-up time.

Please noted, during Power-On-Reset, the \( V_{DD} \) must go higher than \( V_{POR} \) to boot-up the MCU.

![Fig. 1: Power Up Sequence](image)
5.2.1. Timing charts for reset conditions

- **Boot up from LVR detection**

- **Boot up from Watch Dog Time Out**

- **Boot up from Reset Pad reset**
5.3. Data Memory – SRAM

The access of data memory can be byte or bit operation. Besides data storage, the SRAM data memory is also served as data pointer of indirect access method and the stack memory.

The stack memory is defined in the data memory. The stack pointer is defined in the stack pointer register; the depth of stack memory of each processing unit is defined by the user. The arrangement of stack memory fully flexible and can be dynamically adjusted by the user.

For indirect memory access mechanism, the data memory is used as the data pointer to address the data byte. All the data memory could be the data pointer; it's quite flexible and useful to do the indirect memory access. All the 64 bytes data memory of PMS150C can be accessed by indirect access mechanism.

5.4. Oscillator and clock

There are two oscillator circuits provided by PMS150C: internal high RC oscillator (IHRC) and internal low RC oscillator (ILRC), and these two oscillators are enabled or disabled by registers clkmd.4 and clkmd.2 independently. User can choose one of these two oscillators as system clock source and use clkmd register to target the desired frequency as system clock to meet different application.

<table>
<thead>
<tr>
<th>Oscillator Module</th>
<th>Enable/Disable</th>
</tr>
</thead>
<tbody>
<tr>
<td>IHRC</td>
<td>clkmd.4</td>
</tr>
<tr>
<td>ILRC</td>
<td>clkmd.2</td>
</tr>
</tbody>
</table>

5.4.1. Internal High RC oscillator and Internal Low RC oscillator

After boot-up, the IHRC and ILRC oscillators are enabled. The frequency of IHRC can be calibrated to eliminate process variation by ihrcr register; normally it is calibrated to 16MHz. The frequency deviation can be within 2% normally after calibration and it still drifts slightly with supply voltage and operating temperature, the total drift rate is about ±5% for \( V_{DD}=2.0V \sim 5.5V \) and \(-20^\circ C \sim 70^\circ C\) operating conditions. Please refer to the measurement chart for IHRC frequency verse \( V_{DD} \) and IHRC frequency verse temperature.

The frequency of ILRC will vary by process, supply voltage and temperature, please refer to DC specification and do not use for accurate timing application.

5.4.2. IHRC calibration

The IHRC frequency may be different chip by chip due to manufacturing variation, PMS150C provide the IHRC frequency calibration to eliminate this variation, and this function can be selected when compiling user’s program and the command will be inserted into user’s program automatically. The calibration command is shown as below:

\[
\text{ADJUST_IC SYSCALL=IHRC/(p1), IHRC=(p2)MHz, VDD=(p3)V}
\]

Where,

- \( p1=2, 4, 8, 16, 32 \); In order to provide different system clock.
- \( p2=14 \sim 18 \); In order to calibrate the chip to different frequency, 16MHz is the usually one.
- \( p3=2.2 \sim 5.5 \); In order to calibrate the chip under different supply voltage.
5.4.3. IHRC Frequency Calibration and System Clock

During compiling the user program, the options for IHRC calibration and system clock are shown as Table 2:

<table>
<thead>
<tr>
<th>SYSCLK</th>
<th>CLKMD</th>
<th>IHRCR</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>o Set IHRC / 2</td>
<td>= 34h (IHRC / 2)</td>
<td>Calibrated</td>
<td>IHRC calibrated to 16MHz, CLK=8MHz (IHRC/2)</td>
</tr>
<tr>
<td>o Set IHRC / 4</td>
<td>= 14h (IHRC / 4)</td>
<td>Calibrated</td>
<td>IHRC calibrated to 16MHz, CLK=4MHz (IHRC/4)</td>
</tr>
<tr>
<td>o Set IHRC / 8</td>
<td>= 3Ch (IHRC / 8)</td>
<td>Calibrated</td>
<td>IHRC calibrated to 16MHz, CLK=2MHz (IHRC/8)</td>
</tr>
<tr>
<td>o Set IHRC / 16</td>
<td>= 1Ch (IHRC / 16)</td>
<td>Calibrated</td>
<td>IHRC calibrated to 16MHz, CLK=1MHz (IHRC/16)</td>
</tr>
<tr>
<td>o Set IHRC / 32</td>
<td>= 7Ch (IHRC / 32)</td>
<td>Calibrated</td>
<td>IHRC calibrated to 16MHz, CLK=0.5MHz (IHRC/32)</td>
</tr>
<tr>
<td>o Set ILRC</td>
<td>= E4h (ILRC / 1)</td>
<td>Calibrated</td>
<td>IHRC calibrated to 16MHz, CLK=ILRC</td>
</tr>
<tr>
<td>o Disable</td>
<td>No change</td>
<td>No Change</td>
<td>IHRC not calibrated, CLK not changed</td>
</tr>
</tbody>
</table>

Table 2: Options for IHRC Frequency Calibration

Usually, .ADJUST_IC will be the first command after boot up, in order to set the target operating frequency whenever stating the system. The program code for IHRC frequency calibration is executed only one time that occurs in writing the codes into OTP memory; after then, it will not be executed again. If the different option for IHRC calibration is chosen, the system status is also different after boot. The following shows the status of PMS150C for different option:

(1) .ADJUST_IC SYSCLK=IHRC/2, IHRC=16MHz, V_{DD}=5V
   After boot up, CLKMD = 0x34:
   - IHRC frequency is calibrated to 16MHz@V_{DD}=5V and IHRC module is enabled
   - System CLK = IHRC/2 = 8MHz
   - Watchdog timer is disabled, ILRC is enabled, PA5 is in input mode

(2) .ADJUST_IC SYSCLK=IHRC/4, IHRC=16MHz, V_{DD}=3.3V
   After boot, CLKMD = 0x14:
   - IHRC frequency is calibrated to 16MHz@V_{DD}=3.3V and IHRC module is enabled
   - System CLK = IHRC/4 = 4MHz
   - Watchdog timer is disabled, ILRC is enabled, PA5 is in input mode

(3) .ADJUST_IC SYSCLK=IHRC/8, IHRC=16MHz, V_{DD}=2.5V
   After boot, CLKMD = 0x3C:
   - IHRC frequency is calibrated to 16MHz@V_{DD}=2.5V and IHRC module is enabled
   - System CLK = IHRC/8 = 2MHz
   - Watchdog timer is disabled, ILRC is enabled, PA5 is in input mode

(4) .ADJUST_IC SYSCLK=IHRC/16, IHRC=16MHz, V_{DD}=2.2V
   After boot, CLKMD = 0x1C:
   - IHRC frequency is calibrated to 16MHz@V_{DD}=2.2V and IHRC module is enabled
   - System CLK = IHRC/16 = 1MHz
   - Watchdog timer is disabled, ILRC is enabled, PA5 is in input mode
(5) .ADJUST_IC  SYSCLK=IHRC/32, IHRC=16MHz, VDD=5V
After boot, CLKMD = 0x7C:
- IHRC frequency is calibrated to 16MHz@VDD=5V and IHRC module is enabled
- System CLK = IHRC/32 = 500KHz
- Watchdog timer is disabled, ILRC is enabled, PA5 is in input mode

(6) .ADJUST_IC  SYSCLK=ILRC, IHRC=16MHz, VDD=5V
After boot, CLKMD = 0XE4:
- IHRC frequency is calibrated to 16MHz@VDD=5V and IHRC module is disabled
- System CLK = ILRC
- Watchdog timer is disabled, ILRC is enabled, PA5 is input mode

(7) .ADJUST_IC DISABLE
After boot, CLKMD is not changed (Do nothing):
- IHRC is not calibrated.
- System CLK = ILRC or IHRC/64 (by Boot-up_Time)
- Watchdog timer is enabled, ILRC is enabled, PA5 is in input mode

5.4.4. System Clock and LVR levels

The clock source of system clock comes from IHRC or ILRC, the hardware diagram of system clock in the PMS150C is shown as Fig. 2.

![Fig. 2: Options of System Clock](image)

User can choose different operating system clock depends on its requirement; the selected operating system clock should be combined with supply voltage and LVR level to make system stable. The LVR level will be selected during compilation, and the lowest LVR levels can be chosen for different operating frequencies. Please refer to Section 4.1.
5.5. Comparator

One hardware comparator is built inside the PMS150C; Fig. 3 shows its hardware diagram. It can compare signals between two pins or with either internal reference voltage $V_{\text{internal R}}$ or internal band-gap reference voltage. The two signals to be compared, one is the plus input and the other one is the minus input. For the minus input of comparator can be PA3, PA4, Internal band-gap 1.20V, PA6, PA7 or $V_{\text{internal R}}$ selected by bit [3:1] of gpcc register, and the plus input of comparator can be PA4 or $V_{\text{internal R}}$ selected by bit 0 of gpcc register. The output result can be enabled to output to PA0 directly, or sampled by Timer2 clock (TM2_CLK) which comes from Timer2 module. The output can be also inversed the polarity by bit 4 of gpcc register, the comparator output can be used to request interrupt service.

Fig. 3: Hardware diagram of comparator
5.5.1. Internal reference voltage ($V_{\text{internal R}}$)

The internal reference voltage $V_{\text{internal R}}$ is built by series resistance to provide different level of reference voltage, bit 4 and bit 5 of gpcs register are used to select the maximum and minimum values of $V_{\text{internal R}}$ and bit [3:0] of gpcs register are used to select one of the voltage level which is divided-by-16 from the defined maximum level to minimum level. Fig. 4 to Fig. 7 shows four conditions to have different reference voltage $V_{\text{internal R}}$. By setting the gpcs register, the internal reference voltage $V_{\text{internal R}}$ can be ranged from $(1/32)*V_{\text{DD}}$ to $(3/4)*V_{\text{DD}}$.

**Case 1 : gpcs.5=0 & gpcs.4=0**

$$V_{\text{internal R}} = \frac{3}{4}V_{\text{DD}} \sim \frac{1}{4}V_{\text{DD}} + \frac{1}{32}V_{\text{DD}}$$

@ gpcs[3:0] = 1111 ~ gpcs[3:0] = 0000

$$V_{\text{internal R}} = \frac{1}{4}V_{\text{DD}} + \frac{(n+1)}{32}V_{\text{DD}}, n = \text{gpcs[3:0] in decimal}$$

Fig. 4: $V_{\text{internal R}}$ hardware connection if gpcs.5=0 and gpcs.4=0

**Case 2 : gpcs.5=0 & gpcs.4=1**

$$V_{\text{internal R}} = \frac{2}{3}V_{\text{DD}} \sim \frac{1}{24}V_{\text{DD}}$$

@ gpcs[3:0] = 1111 ~ gpcs[3:0] = 0000

$$V_{\text{internal R}} = \frac{(n+1)}{24}V_{\text{DD}}, n = \text{gpcs[3:0] in decimal}$$

Fig. 5: $V_{\text{internal R}}$ hardware connection if gpcs.5=0 and gpcs.4=1
Case 3: gpcs.5=1 & gpcs.4=0

\[ V_{\text{internal R}} = \left( \frac{3}{5} \right) \text{VDD} \sim \left( \frac{1}{5} \right) \text{VDD} + \left( \frac{1}{40} \right) \text{VDD} \]

@ gpcs[3:0] = 1111 ~ gpcs[3:0] = 0000

\[ V_{\text{internal R}} = \frac{1}{5} \times \text{VDD} + \frac{(n+1)}{40} \times \text{VDD}, \ n = \text{gpcs[3:0] in decimal} \]

Fig.6: \( V_{\text{internal R}} \) hardware connection if gpcs.5=1 and gpcs.4=0

Case 4: gpcs.5=1 & gpcs.4=1

\[ V_{\text{internal R}} = \left( \frac{1}{2} \right) \text{VDD} \sim \left( \frac{1}{32} \right) \text{VDD} \]

@ gpcs[3:0] = 1111 ~ gpcs[3:0] = 0000

\[ V_{\text{internal R}} = \frac{(n+1)}{32} \times \text{VDD}, \ n = \text{gpcs[3:0] in decimal} \]

Fig.7: \( V_{\text{internal R}} \) hardware connection if gpcs.5=1 and gpcs.4=1
5.5.2. Using the comparator

Case A:

Choosing PA3 as minus input and $V_{\text{internal R}}$ with $(18/32)*V_{\text{DD}}$ voltage level as plus input. $V_{\text{internal R}}$ is configured as the above Figure “gpcs[5:4] = 2b'00” and gpcs [3:0] = 4b’1001 (n=9) to have $V_{\text{internal R}} = (1/4)V_{\text{DD}} + [(9+1)/32]*V_{\text{DD}} = [(9+9)/32]*V_{\text{DD}} = (18/32)*V_{\text{DD}}$.

\[
gpcs = 0b1_0_00_1001; \quad // \text{ } V_{\text{internal R}} = V_{DD}*(18/32)
\]
\[
gpcc = 0b1_0_0_0_000_0; \quad // \text{ enable comp, - input: PA3, + input: } V_{\text{internal R}}
\]
\[
padier = 0bxxxx_0_xxx; \quad // \text{ disable PA3 digital input to prevent leakage current}
\]

or

$\text{GPCS } V_{DD}*18/32;$

$\text{GPCC } \text{Enable, } N_{PA3}, \text{ P_R;} \quad //\text{ - input: } N_{xx} , \text{ + input: } P_{R}(V_{\text{internal R}})$

$\text{PADIER} = 0bxxxx_0_xxx;$

Case B:

Choosing $V_{\text{internal R}}$ as minus input with $(14/32)*V_{\text{DD}}$ voltage level and PA4 as plus input, the comparator result will be inverted and then output to PA0. $V_{\text{internal R}}$ is configured as the above Figure “gpcs[5:4] = 2b’10” and gpcs [3:0] = 4b’1101 (n=13) to have $V_{\text{internal R}} = (1/5)V_{\text{DD}} + [(13+1)/40]*V_{\text{DD}} = [(13+9)/40]*V_{\text{DD}} = (22/40)*V_{\text{DD}}$.

\[
gpcs = 0b1_0_10_1101; \quad // \text{ output to PA0, } V_{\text{internal R}} = V_{DD}*(22/40)
\]
\[
gpcc = 0b1_0_0_1_011_1; \quad // \text{ Inverse output, - input: } V_{\text{internal R}}, \text{ + input: PA4}
\]
\[
padier = 0bxxx_0_xxxx; \quad // \text{ disable PA4 digital input to prevent leakage current}
\]

or

$\text{GPCS } \text{Output, } V_{DD}^*22/40;$

$\text{GPCC } \text{Enable, Inverse, } N_{R}, \text{ P_PA4}; \quad //\text{ - input: } N_{R}(V_{\text{internal R}}), \text{ + input: } P_{xx}$

$\text{PADIER} = 0bxxx_0_xxxx;$

Note: When selecting output to PA0 output, GPCS will affect the PA3 output function in ICE. Though the IC is fine, be careful to avoid this error during emulation.
5.5.3. Using the comparator and band-gap 1.20V

The internal band-gap module provides a stable 1.20V output, and it can be used to measure the external supply voltage level. The band-gap 1.20V is selected as minus input of comparator and Vinternal R is selected as plus input, the supply voltage of Vinternal R is VDD, the VDD voltage level can be detected by adjusting the voltage level of Vinternal R to compare with band-gap. If N (gpcs[3:0] in decimal) is the number to let Vinternal R closest to band-gap 1.20 volt, the supply voltage VDD can be calculated by using the following equations:

For using Case 1: \( V_{DD} = \left\lceil \frac{32}{N+9} \right\rceil \times 1.20 \text{ volt} \);  
For using Case 2: \( V_{DD} = \left\lceil \frac{24}{N+1} \right\rceil \times 1.20 \text{ volt} \);  
For using Case 3: \( V_{DD} = \left\lceil \frac{40}{N+9} \right\rceil \times 1.20 \text{ volt} \);  
For using Case 4: \( V_{DD} = \left\lceil \frac{32}{N+1} \right\rceil \times 1.20 \text{ volt} \);

\[\text{Case 1:}\]

\$ GPCS VDD*12/40; \quad \text{// 4.0V * 12/40 = 1.2V} \\
$ GPCC Enable, BANDGAP, P_R; \quad \text{// - input: BANDGAP, + input: P_R(V_{\text{internal R}})} \\
....
if  (GPC_Out) \quad \text{// or GPCC.6} 
{ \quad \text{// when V_{DD} > 4V} 
} 
else 
{ \quad \text{// when V_{DD} < 4V} 
}
5.6. 16-bit Timer (Timer16)

PMS150C provide a 16-bit hardware timer (Timer16) and its clock source may come from system clock (CLK), internal high RC oscillator (IHRC), internal low RC oscillator (ILRC), PA0 or PA4. Before sending clock to the 16-bit counter, a pre-scaling logic with divided-by-1, 4, 16 or 64 is selectable for wide range counting. The 16-bit counter performs up-counting operation only, the counter initial values can be stored from data memory by issuing the \texttt{stt16} instruction and the counting values can be loaded to data memory by issuing the \texttt{ldt16} instruction. The interrupt request from Timer16 will be triggered by the selected bit which comes from bit[15:8] of this 16-bit counter, rising edge or falling edge can be optional chosen by register \texttt{integs.4}. The hardware diagram of Timer16 is shown as Fig. 8.

When using the Timer16, the syntax for Timer16 has been defined in the .INC file. There are three parameters to define the Timer16 using; 1\textsuperscript{st} parameter is used to define the clock source of Timer16, 2\textsuperscript{nd} parameter is used to define the pre-scaler and the 3\textsuperscript{rd} one is to define the interrupt source.

\begin{verbatim}
T16M IO_RW 0x06
$ 7~5: STOP, SYSCLK, X, PA4_F, IHRC, X, ILRC, PA0_F // 1\textsuperscript{st} par.
$ 4~3: /1, /4, /16, /64 // 2\textsuperscript{nd} par.
$ 2~0: BIT8, BIT9, BIT10, BIT11, BIT12, BIT13, BIT14, BIT15 // 3\textsuperscript{rd} par.
\end{verbatim}

User can choose the proper parameters of T16M to meet system requirement, examples as below:

\begin{verbatim}
$ T16M SYSCLK, /64, BIT15;
// choose (SYSCLK/64) as clock source, every 2^16 clock to set INTRQ.2=1
// if system clock SYSCLK = IHRC / 2 = 8 MHz
// SYSCLK/64 = 8 MHz/64 = 8 uS, about every 524 mS to generate INTRQ.2=1

$ T16M PA0, /1, BIT8;
// choose PA0 as clock source, every 2^9 to generate INTRQ.2=1
// receiving every 512 times PA0 to generate INTRQ.2=1

$ T16M STOP;
// stop Timer16 counting
\end{verbatim}
5.7. 8-bit timer (Timer2) with PWM generation

One 8-bit hardware timer (Timer2/TM2) with PWM generation is implemented in the PMS150C. Please refer to Fig. 9 shown its hardware diagram, the clock sources of Timer2 may come from system clock, internal high RC oscillator (IHRC) or, internal low RC oscillator (ILRC), PA0 or PA4. Bit[7:4] of register tm2c are used to select the clock source of Timer2. Please notice that if IHRC is selected for Timer2 clock source, the clock sent to Timer2 will keep running when using ICE in halt state. The output of Timer2 can be sent to pin PA3 or PA4, depending on bit [3-2] of tm2c register. A clock pre-scaling module is provided with divided-by-1, 4, 16, and 64 options, controlled by bit [6:5] of tm2s register; one scaling module with divided-by-1~31 is also provided and controlled by bit [4:0] of tm2s register. In conjunction of pre-scaling function and scaling function, the frequency of Timer2 clock (TM2_CLK) can be wide range and flexible.

The Timer2 counter performs 8-bit up-counting operation only; the counter values can be set or read back by tm2ct register. The 8-bit counter will be clear to zero automatically when its values reach for upper bound register, the upper bound register is used to define the period of timer or duty of PWM. There are two operating modes for Timer2: period mode and PWM mode; period mode is used to generate periodical output waveform or interrupt event; PWM mode is used to generate PWM output waveform with optional 6-bit or 8-bit PWM resolution, Fig. 10 shows the timing diagram of Timer2 for both period mode and PWM mode.

Fig. 9: Timer2 hardware diagram
5.7.1. Using the Timer2 to generate periodical waveform

If periodical mode is selected, the duty cycle of output is always 50%; its frequency can be summarized as below:

\[
\text{Frequency of Output} = \frac{Y}{2 \times (K+1) \times S1 \times (S2+1)}
\]

Where,
- \( Y = \text{tm2c}[7:4] \): frequency of selected clock source
- \( K = \text{tm2b}[7:0] \): bound register in decimal
- \( S1 = \text{tm2s}[6:5] \): pre-scalar (1, 4, 16, 64)
- \( S2 = \text{tm2s}[4:0] \): scalar register in decimal (1 ~ 31)

**Example 1:**
- \( \text{tm2c} = 0b0001_1000 \), \( Y=8MHz \)
- \( \text{tm2b} = 0b0111_1111 \), \( K=127 \)
- \( \text{tm2s} = 0b0_00_00000 \), \( S1=1, S2=0 \)
  - frequency of output = \( 8MHz \div \left(2 \times (127+1) \times 1 \times (0+1)\right) = 31.25kHz \)

**Example 2:**
- \( \text{tm2c} = 0b0001_1000 \), \( Y=8MHz \)
- \( \text{tm2b} = 0b0111_1111 \), \( K=127 \)
- \( \text{tm2s}[7:0] = 0b0_11_11111 \), \( S1=64, S2 = 31 \)
  - frequency = \( 8MHz \div (2 \times (127+1) \times 64 \times (31+1)) = 15.25Hz \)

**Example 3:**
- \( \text{tm2c} = 0b0001_1000 \), \( Y=8MHz \)
- \( \text{tm2b} = 0b0000_1111 \), \( K=15 \)
- \( \text{tm2s} = 0b0_00_00000 \), \( S1=1, S2=0 \)
  - frequency = \( 8MHz \div (2 \times (15+1) \times 1 \times (0+1)) = 250kHz \)

**Example 4:**
- \( \text{tm2c} = 0b0001_1000 \), \( Y=8MHz \)
- \( \text{tm2b} = 0b0000_0001 \), \( K=1 \)
- \( \text{tm2s} = 0b0_00_00000 \), \( S1=1, S2=0 \)
  - frequency = \( 8MHz \div (2 \times (1+1) \times 1 \times (0+1)) = 2MHz \)
The sample program for using the Timer2 to generate periodical waveform to PA3 is shown as below:

```c
void FPPA0 (void) {
    // ADJUST_IC SYSCLK=IHRC/2, IHRC=16MHz, VDD=5V
    ...
    tm2ct = 0x0;
    tm2b = 0x7f;
    tm2s = 0b0_00_00001;  // 8-bit PWM, pre-scalar = 1, scalar = 2
    tm2c = 0b0001_10_0_0;  // system clock, output=PA3, period mode
    while(1) {
        nop;
    }
}
```

### 5.7.2. Using the Timer2 to generate 8-bit PWM waveform

If 8-bit PWM mode is selected, it should set \( \text{tm2c}[1]=1 \) and \( \text{tm2s}[7]=0 \), the frequency and duty cycle of output waveform can be summarized as below:

- **Frequency of Output** = \( \frac{Y}{256 \times S1 \times (S2+1)} \)
- **Duty of Output** = \( \frac{K+1}{256} \times 100\% \)

**Where**,

- \( Y = \text{tm2c}[7:4] \) : frequency of selected clock source
- \( K = \text{tm2b}[7:0] \) : bound register in decimal
- \( S1= \text{tm2s}[6:5] \) : pre-scalar (1, 4, 16, 64)
- \( S2 = \text{tm2s}[4:0] \) : scalar register in decimal (1 ~ 31)

**Example 1:**

\[ \begin{align*}
\text{tm2c} &= 0b0001_1010, \ Y=8MHz \\
\text{tm2b} &= 0b0111_1111, \ K=127 \\
\text{tm2s} &= 0b0_00_00000, \ S1=1, \ S2=0 \\
\rightarrow \text{frequency of output} &= 8MHz \div (256 \times 1 \times (0+1)) = 31.25kHz \\
\rightarrow \text{duty of output} &= \frac{(127+1)}{256} \times 100\% = 50\%
\end{align*} \]

**Example 2:**

\[ \begin{align*}
\text{tm2c} &= 0b0001_1010, \ Y=8MHz \\
\text{tm2b} &= 0b0111_1111, \ K=127 \\
\text{tm2s} &= 0b0_11_11111, \ S1=64, \ S2=31 \\
\rightarrow \text{frequency of output} &= 8MHz \div (256 \times 64 \times (31+1)) = 15.25Hz \\
\rightarrow \text{duty of output} &= \frac{(127+1)}{256} \times 100\% = 50\%
\end{align*} \]

**Example 3:**

\[ \begin{align*}
\text{tm2c} &= 0b0001_1010, \ Y=8MHz \\
\text{tm2b} &= 0b1111_1111, \ K=255 \\
\text{tm2s} &= 0b0_00_00000, \ S1=1, \ S2=0 \\
\rightarrow \text{frequency of output} &= 8MHz \div (256 \times 1 \times (0+1)) = 31.25kHz \\
\rightarrow \text{duty of output} &= \frac{(255+1)}{256} \times 100\% = 100\%
\end{align*} \]
Example 4:
\[
\begin{align*}
\text{tm2c} &= 0b0001\_1010, \ Y=8\text{MHz} \\
\text{tm2b} &= 0b0000\_1001, \ K = 9 \\
\text{tm2s} &= 0b0\_00\_00000, \ S1=1, \ S2=0 \\
\rightarrow \ & \text{frequency of output} = 8\text{MHz} \div (256 \times 1 \times (0+1)) = 31.25\text{kHz} \\
\rightarrow \ & \text{duty of output} = [(9+1) \div 256] \times 100% = 3.9\%
\end{align*}
\]

The sample program for using the Timer2 to generate PWM waveform from PA3 is shown as below:

```c
void FPPA0 (void)
{
    .ADJUST_IC SYSCLK=IHRC/2, IHRC=16MHz, VDD=5V
    wdreset;
    tm2ct = 0x0;
    tm2b = 0x7f;
    tm2s = 0b0\_00\_00001; \ // \ 8\text{-}bit \ PWM, \ pre\text{-}scalar = 1, \ scalar = 2
    tm2c = 0b0001\_10\_1\_0; \ // \ system \ clock, \ output=PA3, \ PWM \ mode
    while(1)
    {
        nop;
    }
}
```

5.7.3. Using the Timer2 to generate 6-bit PWM waveform

If 6-bit PWM mode is selected, it should set tm2c[1]=1 and tm2s[7]=1, the frequency and duty cycle of output waveform can be summarized as below:

**Frequency of Output** = \(Y \div [64 \times S1 \times (S2+1)]\)

**Duty of Output** = \([(K+1) \div 64] \times 100\%\)

Where,  
\[
\begin{align*}
\text{tm2c}[7:4] &= Y : \text{frequency of selected clock source} \\
\text{tm2b}[7:0] &= K : \text{bound register in decimal} \\
\text{tm2s}[6:5] &= S1 : \text{pre\text{-}scalar (1, 4, 16, 64)} \\
\text{tm2s}[4:0] &= S2 : \text{scalar register in decimal (1 ~ 31)}
\end{align*}
\]

**Example 1:**
\[
\begin{align*}
\text{tm2c} &= 0b0001\_1010, \ Y=8\text{MHz} \\
\text{tm2b} &= 0b0001\_1111, \ K=31 \\
\text{tm2s} &= 0b1\_00\_00000, \ S1=1, \ S2=0 \\
\rightarrow \ & \text{frequency of output} = 8\text{MHz} \div (64 \times 1 \times (0+1)) = 125\text{kHz} \\
\rightarrow \ & \text{duty} = [(31+1) \div 64] \times 100\% = 50\%
\end{align*}
\]
Example 2:
\[ \text{tm2c} = 0b0001_1010, \ Y=8MHz \]
\[ \text{tm2b} = 0b0001_1111, \ K=31 \]
\[ \text{tm2s} = 0b1_11_1111_1, \ S1=64, \ S2=31 \]
\[ \text{frequency of output} = 8MHz ÷ (64 × 64 × (31+1)) = 61.03 \text{ Hz} \]
\[ \text{duty of output} = [(31+1) ÷ 64] × 100\% = 50\% \]

Example 3:
\[ \text{tm2c} = 0b0001_1010, \ Y=8MHz \]
\[ \text{tm2b} = 0b0011_1111, \ K=63 \]
\[ \text{tm2s} = 0b1_00_00000, \ S1=1, \ S2=0 \]
\[ \text{frequency of output} = 8MHz ÷ (64 × 1 × (0+1)) = 125kHz \]
\[ \text{duty of output} = [(63+1) ÷ 64] × 100\% = 100\% \]

Example 4:
\[ \text{tm2c} = 0b0001_1010, \ Y=8MHz \]
\[ \text{tm2b} = 0b0000_0000, \ K=0 \]
\[ \text{tm2s} = 0b1_00_00000, \ S1=1, \ S2=0 \]
\[ \text{frequency} = 8MHz ÷ (64 × 1 × (0+1)) = 125kHz \]
\[ \text{duty} = [(0+1) ÷ 64] × 100\% =1.5\% \]
5.8. Watchdog Timer

The watchdog timer (WDT) is a counter with clock coming from ILRC and its frequency is about 62KHz@5V. There are 4 different timeout periods of watchdog timer can be chosen by setting the *misc* register, it is:

- 256k ILRC clock period when misc[1:0]=11
- 64k ILRC clock period when misc[1:0]=10
- 16k ILRC clock period when misc[1:0]=01
- 8k ILRC clock period when misc[1:0]=00 (default)

The frequency of ILRC may drift a lot due to the variation of manufacture, supply voltage and temperature; user should reserve guard band for safe operation. WDT can be cleared by power-on-reset or by command *wdreset* at any time. When WDT is timeout, PMS150C will be reset to restart the program execution. The relative timing diagram of watchdog timer is shown as Fig. 11.

![Watch Dog Time Out Sequence](image)

Fig. 11: Sequence of Watch Dog Time Out
5.9. Interrupt

There are four interrupt lines for PMS150C:

- External interrupt PA0
- GPC interrupt
- Timer16 interrupt
- Timer2 interrupt

Every interrupt request line has its own corresponding interrupt control bit to enable or disable it; the hardware diagram of interrupt function is shown as Fig. 12. All the interrupt request flags are set by hardware and cleared by writing `intrq` register. When the request flags are set, it can be rising edge, falling edge or both, depending on the setting of register `integs`. All the interrupt request lines are also controlled by `engint` instruction (enable global interrupt) to enable interrupt operation and `disgint` instruction (disable global interrupt) to disable it. The stack memory for interrupt is shared with data memory and its address is specified by stack register `sp`. Since the program counter is 16 bits width, the bit 0 of stack register `sp` should be kept 0. Moreover, user can use `pushaf` / `popaf` instructions to store or restore the values of `ACC` and `flag` register to / from stack memory.

Since the stack memory is shared with data memory, the stack position and level are arranged by the compiler in Mini-C project. When defining the stack level in ASM project, users should arrange their locations carefully to prevent address conflicts.

![Fig. 12: Hardware diagram of Interrupt controller](image-url)
Once the interrupt occurs, its operation will be:

- The program counter will be stored automatically to the stack memory specified by register `sp`
- New `sp` will be updated to `sp+2`
- Global interrupt will be disabled automatically.
- The next instruction will be fetched from address 0x010.

During the interrupt service routine, the interrupt source can be determined by reading the `intrq` register.

Note: Even if `INTEN=0`, `INTRQ` will be still triggered by the interrupt source.

After finishing the interrupt service routine and issuing the `reti` instruction to return back, its operation will be:

- The program counter will be restored automatically from the stack memory specified by register `sp`
- New `sp` will be updated to `sp-2`
- Global interrupt will be enabled automatically.
- The next instruction will be the original one before interrupt.

User must reserve enough stack memory for interrupt, two bytes stack memory for one level interrupt and four bytes for two levels interrupt. And so on, two bytes stack memory is for `pushaf`. For interrupt operation, the following sample program shows how to handle the interrupt, noticing that it needs four bytes stack memory to handle interrupt and `pushaf`.

```c
void FPPA0 (void)
{
...
$ INTEN PA0; // INTEN =1; interrupt request when PA0 level changed
INTRQ = 0; // clear INTRQ
ENGINT // global interrupt enable
...
DISGINT // global interrupt disable
...
}
```
void Interrupt (void) // interrupt service routine
{
    PUSHAF // store ALU and FLAG register

    // If INTEN.PA0 will be opened and closed dynamically,
    // user can judge whether INTEN.PA0 =1 or not.
    // Example:  If (INTEN.PA0 && INTRQ.PA0) {...}

    // If INTEN.PA0 is always enable,
    // user can omit the INTEN.PA0 judgement to speed up interrupt service routine.

    If (INTRQ.PA0)
    {
        // Here for PA0 interrupt service routine
        INTRQ.PA0 = 0; // Delete corresponding bit (take PA0 for example)
        ...
    }
    ...
    // X : INTRQ = 0;  // It is not recommended to use INTRQ = 0 to clear all at the end of
    // the interrupt service routine.
    // It may accidentally clear out the interrupts that have just occurred
    // and are not yet processed.
    POPAF // restore ALU and FLAG register
}
5.10. Power-Save and Power-Down

There are three operational modes defined by hardware: ON mode, Power-Save mode and Power-Down modes. ON mode is the state of normal operation with all functions ON, Power-Save mode ("stopexe") is the state to reduce operating current and CPU keeps ready to continue, Power-Down mode ("stopsys") is used to save power deeply. Therefore, Power-Save mode is used in the system which needs low operating power with wake-up occasionally and Power-Down mode is used in the system which needs power down deeply with seldom wake-up. Table 3 shows the differences in oscillator modules between Power-Save mode ("stopexe") and Power-Down mode ("stopsys").

<table>
<thead>
<tr>
<th>Differences in oscillator modules between STOPSYS and STOPEXE</th>
</tr>
</thead>
<tbody>
<tr>
<td>IHRC</td>
</tr>
<tr>
<td>STOPSYS</td>
</tr>
<tr>
<td>STOPEXE</td>
</tr>
</tbody>
</table>

Table 3: Differences in oscillator modules between STOPSYS and STOPEXE

5.10.1. Power-Save mode ("stopexe")

Using "stopexe" instruction to enter the Power-Save mode, only system clock is disabled, remaining all the oscillator modules be active. For CPU, it stops executing; however, for Timer16, counter keep counting if its clock source is not the system clock. The wake-up sources for "stopexe" can be IO-toggle or Timer16 counts to set values when the clock source of Timer16 is IHRC or ILRC modules. Wake-up from input pins can be considered as a continuation of normal execution, the detail information for Power-Save mode shown below:

- IHRC and ILRC oscillator modules: No change, keep active if it was enabled.
- System clock: Disable, therefore, CPU stops execution.
- OTP memory is turned off.
- Timer16, Timer2: Stop counting if system clock is selected by clock source or the corresponding oscillator module is disabled; otherwise, it keeps counting.
- Wake-up sources: IO toggle in digital mode (PxDIR bit is 1) or Timer16 or Timer2.

The watchdog timer must be disabled before issuing the "stopexe" command, the example is shown as below:

```c
CLKMD.En_WatchDog = 0;  // disable watchdog timer
stopexe;
....                    // power saving
Wdreset;
CLKMD.En_WatchDog = 1;  // enable watchdog timer
```
Another example shows how to use Timer16 to wake-up from "stopexe":

```c
$ T16M ILRC, /1, BIT8 // Timer16 setting
...
WORD  count  =  0;
STT16  count;
stopexe;
...
```

The initial counting value of Timer16 is zero and the system will be waken up after the Timer16 counts 256 ILRC clocks.

5.10.2. Power-Down mode ("stopsys")

Power-Down mode is the state of deeply power-saving with turning off all the oscillator modules. By using the "stopsys" instruction, this chip will be put on Power-Down mode directly. The following shows the internal status of PMS150C in detail when "stopsys" command is issued:

- All the oscillator modules are turned off.
- OTP memory is turned off.
- The contents of SRAM and registers remain unchanged.
- Wake-up sources: IO toggle in digital mode (PxDIR bit is 1)

Wake-up from input pins can be considered as a continuation of normal execution. To minimize power consumption, all the I/O pins should be carefully manipulated before entering power-down mode. The reference sample program for power down is shown as below:

```c
CMKMD  =  0xF4;  // Change clock from IHRC to ILRC, disable watchdog timer
CLKMD.4 =  0;    // disable IHRC
...
while (1)
{
    STOPSYS;        // enter power-down
    if (...) break; // if wakeup happen and check OK, then return to high speed,
    // else stay in power-down mode again.
}
CLKMD  =  0x34;  // Change clock from ILRC to IHRC/2
```
5.10.3. Wake-up

After entering the Power-Down or Power-Save modes, the PMS150C can be resumed to normal operation by toggling IO pins. Timer16, Timer2 interrupt is available for Power-Save mode ONLY. Table 4 shows the differences in wake-up sources between STOPSYS and STOPEXE.

<table>
<thead>
<tr>
<th>Differences in wake-up sources between STOPSYS and STOPEXE</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
</tr>
<tr>
<td>STOPSYS</td>
</tr>
<tr>
<td>STOPEXE</td>
</tr>
</tbody>
</table>

Table 4: Differences in wake-up sources between Power-Save mode and Power-Down mode

When using the IO pins to wake-up the PMS150C, registers `padier` should be properly set to enable the wake-up function for every corresponding pin. The time for normal wake-up is about 2048 ILRC clocks counting from wake-up event; fast wake-up can be selected to reduce the wake-up time by `misc` register, and the time for fast wake-up is 32 ILRC clocks from IO toggling.

<table>
<thead>
<tr>
<th>Suspend mode</th>
<th>Wake-up mode</th>
<th>Wake-up time ( t_{WUP} ) from IO toggle</th>
</tr>
</thead>
<tbody>
<tr>
<td>STOPEXE</td>
<td>fast wake-up</td>
<td>( 32 \times T_{ILRC} ) Where ( T_{ILRC} ) is the time period of ILRC</td>
</tr>
<tr>
<td>STOPSYS</td>
<td></td>
<td></td>
</tr>
<tr>
<td>STOPEXE</td>
<td>normal wake-up</td>
<td>( 2048 \times T_{ILRC} ) Where ( T_{ILRC} ) is the clock period of ILRC</td>
</tr>
<tr>
<td>STOPSYS</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
5.11. IO Pins

Other than PA5, all the pins can be independently set into two states output or input by configuring the data registers (pa), control registers (pac) and pull-high registers (paph). All these pins have Schmitt-trigger input buffer and output driver with CMOS level. When it is set to output low, the pull-up resistor is turned off automatically. If user wants to read the pin state, please notice that it should be set to input mode before reading the data port; if user reads the data port when it is set to output mode, the reading data comes from data register, NOT from IO pad. As an example, Table 5 shows the configuration table of bit 0 of port A. The hardware diagram of IO buffer is also shown as Fig. 13.

<table>
<thead>
<tr>
<th>pa.0</th>
<th>pac.0</th>
<th>paph.0</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>0</td>
<td>0</td>
<td>Input without pull-up resistor</td>
</tr>
<tr>
<td>X</td>
<td>0</td>
<td>1</td>
<td>Input with pull-up resistor</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>X</td>
<td>Output low without pull-up resistor</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>Output high without pull-up resistor</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>Output high with pull-up resistor</td>
</tr>
</tbody>
</table>

Table 5: PA0 Configuration Table

Most IOs can be adjusted their Driving or Sinking current capability to Normal or Low by code option Drive.

Other than PA5, all the IO pins have the same structure; PA5 can be open-drain ONLY when setting to output mode (without Q1). When PMS150C is put in power-down or power-save mode, every pin can be used to wake-up system by toggling its state. Therefore, those pins needed to wake-up system must be set to input mode and set the corresponding bits of registers padier to high. The same reason, padier.0 should be set to high when PA0 is used as external interrupt pin.
5.12. Reset

There are many causes to reset the PMS150C, once reset is asserted, all the registers in PMS150C will be set to default values, system should be restarted once abnormal cases happen, or by jumping program counter to address 'h0. The data memory is in uncertain state when reset comes from power-up and LVR; however, the content will be kept when reset comes from PRST# pin or WDT timeout.

6. IO Registers

6.1. ACC Status Flag Register (flag), IO address = 0x00

<table>
<thead>
<tr>
<th>Bit</th>
<th>Reset</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7 - 4</td>
<td>-</td>
<td>-</td>
<td>Reserved. These four bits are “1” when read.</td>
</tr>
<tr>
<td>3</td>
<td>-</td>
<td>R/W</td>
<td>OV (Overflow). This bit is set whenever the sign operation is overflow.</td>
</tr>
<tr>
<td>2</td>
<td>-</td>
<td>R/W</td>
<td>AC (Auxiliary Carry). There are two conditions to set this bit, the first one is carry out of low nibble in addition operation, and the other one is borrow from the high nibble into low nibble in subtraction operation.</td>
</tr>
<tr>
<td>1</td>
<td>-</td>
<td>R/W</td>
<td>C (Carry). There are two conditions to set this bit, the first one is carry out in addition operation, and the other one is borrow in subtraction operation. Carry is also affected by shift with carry instruction.</td>
</tr>
<tr>
<td>0</td>
<td>-</td>
<td>R/W</td>
<td>Z (Zero). This bit will be set when the result of arithmetic or logic operation is zero; Otherwise, it is cleared.</td>
</tr>
</tbody>
</table>

6.2. Stack Pointer Register (sp), IO address = 0x02

<table>
<thead>
<tr>
<th>Bit</th>
<th>Reset</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7 - 0</td>
<td>-</td>
<td>R/W</td>
<td>Stack Pointer Register. Read out the current stack pointer, or write to change the stack pointer. Please notice that bit 0 should be kept 0 due to program counter is 16 bits.</td>
</tr>
</tbody>
</table>

6.3. Clock Mode Register (clkmd), IO address = 0x03

<table>
<thead>
<tr>
<th>Bit</th>
<th>Reset</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7 - 5</td>
<td>111</td>
<td>R/W</td>
<td>System clock selection:</td>
</tr>
<tr>
<td></td>
<td>Type 0, clkmd[3]=0</td>
<td>Type 1, clkmd[3]=1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>000: IHRC÷ 4</td>
<td>000: IHRC÷ 16</td>
<td></td>
</tr>
<tr>
<td></td>
<td>001: IHRC÷ 2</td>
<td>001: IHRC÷ 8</td>
<td></td>
</tr>
<tr>
<td></td>
<td>01x: reserved</td>
<td>010: ILRC÷ 16 (ICE does NOT Support.)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>10x: reserved</td>
<td>011: IHRC÷ 32</td>
<td></td>
</tr>
<tr>
<td></td>
<td>110: ILRC÷ 4</td>
<td>100: IHRC÷ 64</td>
<td></td>
</tr>
<tr>
<td></td>
<td>111: ILRC (default)</td>
<td>1xx: reserved</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>1</td>
<td>R/W</td>
<td>IHRC oscillator Enable. 0 / 1: disable / enable</td>
</tr>
<tr>
<td>3</td>
<td>0</td>
<td>RW</td>
<td>Clock Type Select. This bit is used to select the clock type in bit [7:5]. 0 / 1: Type 0 / Type 1</td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>R/W</td>
<td>ILRC Enable. 0 / 1: disable / enable</td>
</tr>
<tr>
<td></td>
<td>If ILRC is disabled, watchdog timer is also disabled.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>R/W</td>
<td>Watch Dog Enable. 0 / 1: disable / enable</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>R/W</td>
<td>Pin PA5/PRST# function. 0 / 1: PA5 / PRST#</td>
</tr>
</tbody>
</table>
6.4. Interrupt Enable Register (*inten*), IO address = 0x04

<table>
<thead>
<tr>
<th>Bit</th>
<th>Reset</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7,5,3,1</td>
<td>-</td>
<td>-</td>
<td>Reserved.</td>
</tr>
<tr>
<td>6</td>
<td>-</td>
<td>R/W</td>
<td>Enable interrupt from Timer2. 0 / 1: disable / enable.</td>
</tr>
<tr>
<td>4</td>
<td>-</td>
<td>R/W</td>
<td>Enable interrupt from comparator. 0 / 1: disable / enable.</td>
</tr>
<tr>
<td>2</td>
<td>-</td>
<td>R/W</td>
<td>Enable interrupt from Timer16 overflow. 0 / 1: disable / enable.</td>
</tr>
<tr>
<td>0</td>
<td>-</td>
<td>R/W</td>
<td>Enable interrupt from PA0. 0 / 1: disable / enable.</td>
</tr>
</tbody>
</table>

6.5. Interrupt Request Register (*intrq*), IO address = 0x05

<table>
<thead>
<tr>
<th>Bit</th>
<th>Reset</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7,5,3,1</td>
<td>-</td>
<td>-</td>
<td>Reserved.</td>
</tr>
<tr>
<td>6</td>
<td>-</td>
<td>R/W</td>
<td>Interrupt Request from Timer2, this bit is set by hardware and cleared by software. 0 / 1: No request / Request</td>
</tr>
<tr>
<td>4</td>
<td>-</td>
<td>R/W</td>
<td>Interrupt Request from comparator, this bit is set by hardware and cleared by software. 0 / 1: No request / Request</td>
</tr>
<tr>
<td>2</td>
<td>-</td>
<td>R/W</td>
<td>Interrupt Request from Timer16, this bit is set by hardware and cleared by software. 0 / 1: No request / Request</td>
</tr>
<tr>
<td>0</td>
<td>-</td>
<td>R/W</td>
<td>Interrupt Request from pin PA0, this bit is set by hardware and cleared by software. 0 / 1: No request / Request</td>
</tr>
</tbody>
</table>

6.6. Timer 16 mode Register (*t16m*), IO address = 0x06

<table>
<thead>
<tr>
<th>Bit</th>
<th>Reset</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7 - 5</td>
<td>000</td>
<td>R/W</td>
<td>Timer Clock source selection</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>000: Timer 16 is disabled</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>001: CLK (system clock)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>010: reserved</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>011: PA4 falling edge (from external pin)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>100: IHRC</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>101: reserved</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>110: ILRC</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>111: PA0 falling edge (from external pin)</td>
</tr>
<tr>
<td>4 - 3</td>
<td>00</td>
<td>R/W</td>
<td>Internal clock divider.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00: + 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>01: + 4</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10: + 16</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11: + 64</td>
</tr>
<tr>
<td>2 - 0</td>
<td>000</td>
<td>R/W</td>
<td>Interrupt source selection. Interrupt event happens when selected bit is changed.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0 : bit 8 of Timer16</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1 : bit 9 of Timer16</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2 : bit 10 of Timer16</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>3 : bit 11 of Timer16</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>4 : bit 12 of Timer16</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>5 : bit 13 of Timer16</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>6 : bit 14 of Timer16</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>7 : bit 15 of Timer16</td>
</tr>
</tbody>
</table>
### 6.7. External Oscillator setting Register (eoscr, write only), IO address = 0x0a

<table>
<thead>
<tr>
<th>Bit</th>
<th>Reset</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7 - 1</td>
<td>-</td>
<td>-</td>
<td>Reserved. Please keep 0.</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>WO</td>
<td>Power-down the LVR hardware modules. 0 / 1: normal / power-down.</td>
</tr>
</tbody>
</table>

### 6.8. Interrupt Edge Select Register (integs), IO address = 0x0c

<table>
<thead>
<tr>
<th>Bit</th>
<th>Reset</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7 - 6</td>
<td>00</td>
<td>WO</td>
<td>Comparator edge selection.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00 : both rising edge and falling edge to trigger interrupt</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>01 : rising edge to trigger interrupt</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10 : falling edge to trigger interrupt</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11 : reserved.</td>
</tr>
<tr>
<td>5</td>
<td>-</td>
<td>-</td>
<td>Reserved. Please keep 0.</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
<td>WO</td>
<td>Timer16 edge selection.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0 : rising edge to trigger interrupt</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1 : falling edge to trigger interrupt</td>
</tr>
<tr>
<td>3 - 2</td>
<td>-</td>
<td>-</td>
<td>Reserved.</td>
</tr>
<tr>
<td>1 - 0</td>
<td>00</td>
<td>WO</td>
<td>PA0 edge selection.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00 : both rising edge and falling edge to trigger interrupt</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>01 : rising edge to trigger interrupt</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10 : falling edge to trigger interrupt</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11 : reserved.</td>
</tr>
</tbody>
</table>

### 6.9. Port A Digital Input Enable Register (padier), IO address = 0x0d

<table>
<thead>
<tr>
<th>Bit</th>
<th>Reset</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7 - 3</td>
<td>1111</td>
<td>WO</td>
<td>Enable PA7<del>PA3 wake up event. 1 / 0 : enable / disable. These bits can be set to low to disable wake up from PA7</del>PA3 toggling.</td>
</tr>
<tr>
<td>2 - 1</td>
<td>-</td>
<td>-</td>
<td>Reserved.</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>WO</td>
<td>Enable PA0 wake up event and interrupt request. 1 / 0 : enable / disable. This bit can be set to low to disable wake up from PA0 toggling and interrupt request from this pin.</td>
</tr>
</tbody>
</table>

### 6.10. Port A Data Registers (pa), IO address = 0x10

<table>
<thead>
<tr>
<th>Bit</th>
<th>Reset</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7 - 0</td>
<td>8'h00</td>
<td>R/W</td>
<td>Data registers for Port A.</td>
</tr>
</tbody>
</table>

### 6.11. Port A Control Registers (pac), IO address = 0x11

<table>
<thead>
<tr>
<th>Bit</th>
<th>Reset</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7 - 0</td>
<td>8'h00</td>
<td>R/W</td>
<td>Port A control registers. This register is used to define input mode or output mode for each corresponding pin of port A. 0 / 1: input / output.</td>
</tr>
</tbody>
</table>

### 6.12. Port A Pull-High Registers (paph), IO address = 0x12

<table>
<thead>
<tr>
<th>Bit</th>
<th>Reset</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7 - 0</td>
<td>8'h00</td>
<td>R/W</td>
<td>Port A pull-high registers. This register is used to enable the internal pull-high device on each corresponding pin of port A. 0 / 1: disable / enable</td>
</tr>
</tbody>
</table>
### 6.13. MISC Register (misc), IO address = 0x1b

<table>
<thead>
<tr>
<th>Bit</th>
<th>Reset</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-6</td>
<td>-</td>
<td>-</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
| 5   | 0     | WO  | Enable fast Wake up.  
   0: Normal wake up.  
   - The wake-up time is 2048 ILRC clocks if normal boot up is selected.  
   - The wake-up time is 32 ILRC clocks if fast boot up is selected.  
   1: Fast wake up.  
   - The wake-up time is 32 ILRC clocks for both normal boot up and fast boot up. |
| 4   | -     | -   | Reserved    |
| 3   | 0     | WO  | Reserved    |
| 2   | 0     | WO  | Disable LVR function.  
   0 / 1 : Enable / Disable |
| 1-0 | 00    | WO  | Watch dog time out period  
   00: 8k ILRC clock period  
   01: 16k ILRC clock period  
   10: 64k ILRC clock period  
   11: 256k ILRC clock period |

### 6.14. Comparator Control Register (gpcc), IO address = 0x1A

<table>
<thead>
<tr>
<th>Bit</th>
<th>Reset</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
</table>
| 7   | 0     | R/W | Enable comparator.  
   0 / 1 : disable / enable  
   - When this bit is set to enable, please also set the corresponding analog input pins to be digital disable to prevent IO leakage. |
| 6   | -     | RO  | Comparator result of comparator.  
   0: plus input < minus input  
   1: plus input > minus input |
| 5   | 0     | R/W | Select whether the comparator result output will be sampled by TM2_CLK?  
   0: result output NOT sampled by TM2_CLK  
   1: result output sampled by TM2_CLK |
| 4   | 0     | R/W | Inverse the polarity of result output of comparator.  
   0: polarity is NOT inversed.  
   1: polarity is inversed. |
| 3-1 | 00    | R/W | Selection the minus input (-) of comparator.  
   000 : PA3  
   001 : PA4  
   010 : Internal 1.20 volt band-gap reference voltage  
   011 : $V_{\text{internal}}$  
   100 : PA6 (not for 5S-I-S0xx)  
   101 : PA7 (not for 5S-I-S0xx)  
   11X : reserved |
| 0   | 0     | R/W | Selection the plus input (+) of comparator.  
   0 : $V_{\text{internal}}$  
   1 : PA4 |
### 6.15. Comparator Selection Register (gpcs), IO address = 0x1E

<table>
<thead>
<tr>
<th>Bit</th>
<th>Reset</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>0</td>
<td>WO</td>
<td>Comparator output enable (to PA0). 0 / 1 : disable / enable (Please avoid this situation: GPCS will affect the PA3 output function when selecting output to PA0 output in ICE.)</td>
</tr>
<tr>
<td>6</td>
<td>0</td>
<td>WO</td>
<td>Wakeup by comparator enable. 0 / 1 : disable / enable</td>
</tr>
<tr>
<td>5</td>
<td>0</td>
<td>WO</td>
<td>Selection of high range of comparator.</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
<td>WO</td>
<td>Selection of low range of comparator.</td>
</tr>
<tr>
<td>3 - 0</td>
<td>0000</td>
<td>WO</td>
<td>Selection the voltage level of comparator. 0000 (lowest) ~ 1111 (highest)</td>
</tr>
</tbody>
</table>

### 6.16. Timer2 Control Register (tm2c), IO address = 0x1C

<table>
<thead>
<tr>
<th>Bit</th>
<th>Reset</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7 - 4</td>
<td>0000</td>
<td>RW</td>
<td>Timer2 clock selection. 0000 : disable 0001 : CLK 0010 : IHRC 0011 : reserved 0100 : ILRC 0101 : comparator output 1000 : PA0 (rising edge) 1001 : ~PA0 (falling edge) 1100 : PA4 (rising edge) 1101 : ~PA4 (falling edge) Others: reserved Notice: In ICE mode and IHRC is selected for Timer2 clock, the clock sent to Timer2 does NOT be stopped, Timer2 will keep counting when ICE is in halt state.</td>
</tr>
<tr>
<td>3 - 2</td>
<td>00</td>
<td>RW</td>
<td>Timer2 output selection. 00 : disable 01 : reserved 10 : PA3 11 : PA4 (not for 5S-I-S0xx)</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>RW</td>
<td>Timer2 mode selection. 0 / 1 : period mode / PWM mode</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>RW</td>
<td>Enable to inverse the polarity of Timer2 output. 0 / 1 : disable / enable</td>
</tr>
</tbody>
</table>

### 6.17. Timer2 Counter Register (tm2ct), IO address = 0x1D

<table>
<thead>
<tr>
<th>Bit</th>
<th>Reset</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7 - 0</td>
<td>0x00</td>
<td>RW</td>
<td>Bit [7:0] of Timer2 counter register.</td>
</tr>
</tbody>
</table>
### 6.18. Timer2 Bound Register (*tm2b*), IO address = 0x09

<table>
<thead>
<tr>
<th>Bit</th>
<th>Reset</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>0x00</td>
<td>WO</td>
<td>Timer2 bound register.</td>
</tr>
</tbody>
</table>

### 6.19. Timer2 Scalar Register (*tm2s*), IO address = 0x17

<table>
<thead>
<tr>
<th>Bit</th>
<th>Reset</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>0</td>
<td>WO</td>
<td>PWM resolution selection.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0 : 8-bit</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1 : 6-bit</td>
</tr>
<tr>
<td>6 - 5</td>
<td>00</td>
<td>WO</td>
<td>Timer2 clock pre-scalar.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00 : ÷ 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>01 : ÷ 4</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10 : ÷ 16</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11 : ÷ 64</td>
</tr>
<tr>
<td>4 - 0</td>
<td>0000</td>
<td>WO</td>
<td>Timer2 clock scalar.</td>
</tr>
</tbody>
</table>
7. Instructions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ACC</td>
<td>Accumulator ( Abbreviation of accumulator )</td>
</tr>
<tr>
<td>a</td>
<td>Accumulator ( Symbol of accumulator in program )</td>
</tr>
<tr>
<td>sp</td>
<td>Stack pointer</td>
</tr>
<tr>
<td>flag</td>
<td>ACC status flag register</td>
</tr>
<tr>
<td>I</td>
<td>Immediate data</td>
</tr>
<tr>
<td>&amp;</td>
<td>Logical AND</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>←</td>
<td>Movement</td>
</tr>
<tr>
<td>^</td>
<td>Exclusive logic OR</td>
</tr>
<tr>
<td>+</td>
<td>Add</td>
</tr>
<tr>
<td>−</td>
<td>Subtraction</td>
</tr>
<tr>
<td>~</td>
<td>NOT (logical complement, 1’s complement)</td>
</tr>
<tr>
<td>T</td>
<td>NEG (2’s complement)</td>
</tr>
<tr>
<td>OV</td>
<td>Overflow (The operational result is out of range in signed 2's complement number system)</td>
</tr>
<tr>
<td>Z</td>
<td>Zero (If the result of ALU operation is zero, this bit is set to 1)</td>
</tr>
<tr>
<td>C</td>
<td>Carry (The operational result is to have carry out for addition or to borrow carry for subtraction in unsigned number system)</td>
</tr>
<tr>
<td>AC</td>
<td>Auxiliary Carry (If there is a carry out from low nibble after the result of ALU operation, this bit is set to 1)</td>
</tr>
<tr>
<td>word</td>
<td>Only addressed in 0<del>0x1F (0</del>31) is allowed</td>
</tr>
<tr>
<td>M.n</td>
<td>Only addressed in 0<del>0xF (0</del>15) is allowed</td>
</tr>
<tr>
<td>IO.n</td>
<td>The bit of register</td>
</tr>
</tbody>
</table>
7.1. Data Transfer Instructions

<table>
<thead>
<tr>
<th>Command</th>
<th>Description</th>
<th>Example</th>
<th>Result</th>
<th>Affected Flags</th>
</tr>
</thead>
<tbody>
<tr>
<td>mov a, l</td>
<td>Move immediate data into ACC.</td>
<td>mov a, 0x0f;</td>
<td>a ← 0fh;</td>
<td>N Z N C N AC N OV</td>
</tr>
<tr>
<td>mov M, a</td>
<td>Move data from ACC into memory</td>
<td>mov MEM, a;</td>
<td>MEM ← a</td>
<td>N Z N C N AC N OV</td>
</tr>
<tr>
<td>mov a, M</td>
<td>Move data from memory into ACC</td>
<td>mov a, MEM;</td>
<td>a ← MEM; Flag Z is set when MEM is zero.</td>
<td>Y Z N C N AC N OV</td>
</tr>
<tr>
<td>mov a, IO</td>
<td>Move data from IO into ACC</td>
<td>mov a, pa;</td>
<td>a ← pa; Flag Z is set when pa is zero.</td>
<td>Y Z N C N AC N OV</td>
</tr>
<tr>
<td>mov IO, a</td>
<td>Move data from ACC into IO</td>
<td>mov pa, a;</td>
<td>pa ← a</td>
<td>N Z N C N AC N OV</td>
</tr>
<tr>
<td>ldt16 word</td>
<td>Move 16-bit counting values in Timer16 to memory in word.</td>
<td>ldt16 word;</td>
<td>word ← 16-bit timer</td>
<td>N Z N C N AC N OV</td>
</tr>
</tbody>
</table>

Application Example:

```
word     T16val ;      // declare a RAM word
...
clear    lb@ T16val ;   // clear T16val (LSB)
clear    hb@ T16val ;   // clear T16val (MSB)
stt16    T16val ;       // initial T16 with 0
...
set1     t16m.5 ;       // enable Timer16
...
set0     t16m.5 ;       // disable Timer16
ldt16    T16val ;       // save the T16 counting value to T16val
...```

------------------------------------------------------------------------------------------------------------------------
### stt16 word

Store 16-bit data from memory in word to Timer16.

**Example:**
```plaintext
stt16 word;
```

**Result:**
16-bit timer ← word

**Affected flags:** <N> Z <N> C <N> AC <N> OV

**Application Example:**

```
word T16val ; // declare a RAM word
...
mov a, 0x34 ;
mov lb@ T16val , a ; // move 0x34 to T16val (LSB)
mov a, 0x12 ;
mov hb@ T16val , a ; // move 0x12 to T16val (MSB)
stt16 T16val ; // initial T16 with 0x1234
...
```

### idxm a, index

Move data from specified memory to ACC by indirect method. It needs 2T to execute this instruction.

**Example:**
```plaintext
idxm a, index;
```

**Result:**

a ← [index], where index is declared by word.

**Affected flags:** <N> Z <N> C <N> AC <N> OV

**Application Example:**

```
word RAMIndex ; // declare a RAM pointer
...
mov a, 0x5B ; // assign pointer to an address (LSB)
mov lb@RAMIndex, a ; // save pointer to RAM (LSB)
mov a, 0x00 ; // assign 0x00 to an address (MSB), should be 0
mov hb@RAMIndex, a ; // save pointer to RAM (MSB)
...
idxm a, RAMIndex ; // move memory data in address 0x5B to ACC
```
**Idxm** index, a

Move data from ACC to specified memory by indirect method. It needs 2T to execute this instruction.

- **Example:** `Idxm` index, a;
- **Result:** `[index] ← a;` where index is declared by word.
- **Affected flags:** `N`, `Z`, `C`, `AC`, `OV`

**Application Example:**

```plaintext
word    RAMIndex ;     // declare a RAM pointer
...
mov     a, 0x5B ;      // assign pointer to an address (LSB)
mov     lb@RAMIndex, a ;  // save pointer to RAM (LSB)
mov     a, 0x00 ;      // assign 0x00 to an address (MSB), should be 0
mov     hb@RAMIndex, a ;  // save pointer to RAM (MSB)
...
mov     a, 0xA5 ;      // move 0xA5 to memory in address 0x5B
Idxm    RAMIndex, a ;  // move to memory
```

**Xch M**

Exchange data between ACC and memory

- **Example:** `Xch MEM ;`
- **Result:** `MEM ← a, a ← MEM`
- **Affected flags:** `N`, `Z`, `C`, `AC`, `OV`

**Pushaf**

Move the ACC and flag register to memory that address specified in the stack pointer.

- **Example:** `Pushaf ;`
- **Result:** `sp ← sp + 2 ;`
- **Affected flags:** `N`, `Z`, `C`, `AC`, `OV`

**Application Example:**

```plaintext
.romadr 0x10 ;       // ISR entry address
Pushaf ;            // put ACC and flag into stack memory
...
Popaf ;             // restore ACC and flag from stack memory
Reti ;             // return from interrupt
```

**Popaf**

Restore ACC and flag from the memory which address is specified in the stack pointer.

- **Example:** `Popaf ;`
- **Result:** `sp ← sp - 2 ;`
- **Affected flags:** `Y`, `Y`, `C`, `AC`, `OV`
7.2. Arithmetic Operation Instructions

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Description</th>
<th>Example</th>
<th>Result</th>
<th>Affected Flags</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>add a, I</strong></td>
<td>Add immediate data with ACC, then put result into ACC</td>
<td><code>add a, 0x0f;</code></td>
<td><code>a ← a + 0fh</code></td>
<td><img src="example-flags" alt="Flags" /></td>
</tr>
<tr>
<td><strong>add a, M</strong></td>
<td>Add data in memory with ACC, then put result into ACC</td>
<td><code>add a, MEM;</code></td>
<td><code>a ← a + MEM</code></td>
<td><img src="example-flags" alt="Flags" /></td>
</tr>
<tr>
<td><strong>add M, a</strong></td>
<td>Add data in memory with ACC, then put result into memory</td>
<td><code>add MEM, a;</code></td>
<td><code>MEM ← a + MEM</code></td>
<td><img src="example-flags" alt="Flags" /></td>
</tr>
<tr>
<td><strong>addc a, M</strong></td>
<td>Add data in memory with ACC and carry bit, then put result into ACC</td>
<td><code>addc a, MEM;</code></td>
<td><code>a ← a + MEM + C</code></td>
<td><img src="example-flags" alt="Flags" /></td>
</tr>
<tr>
<td><strong>addc M, a</strong></td>
<td>Add data in memory with ACC and carry bit, then put result into memory</td>
<td><code>addc MEM, a;</code></td>
<td><code>MEM ← a + MEM + C</code></td>
<td><img src="example-flags" alt="Flags" /></td>
</tr>
<tr>
<td><strong>addc a</strong></td>
<td>Add carry with ACC, then put result into ACC</td>
<td><code>addc a;</code></td>
<td><code>a ← a + C</code></td>
<td><img src="example-flags" alt="Flags" /></td>
</tr>
<tr>
<td><strong>addc M</strong></td>
<td>Add carry with memory, then put result into memory</td>
<td><code>addc MEM;</code></td>
<td><code>MEM ← MEM + C</code></td>
<td><img src="example-flags" alt="Flags" /></td>
</tr>
<tr>
<td><strong>sub a, I</strong></td>
<td>Subtraction immediate data from ACC, then put result into ACC.</td>
<td><code>sub a, 0x0f;</code></td>
<td><code>a ← a - 0fh (a + [2’s complement of 0fh])</code></td>
<td><img src="example-flags" alt="Flags" /></td>
</tr>
<tr>
<td><strong>sub a, M</strong></td>
<td>Subtraction data in memory from ACC, then put result into ACC</td>
<td><code>sub a, MEM;</code></td>
<td><code>a ← a - MEM (a + [2’s complement of M])</code></td>
<td><img src="example-flags" alt="Flags" /></td>
</tr>
<tr>
<td><strong>sub M, a</strong></td>
<td>Subtraction data in ACC from memory, then put result into memory</td>
<td><code>sub MEM, a;</code></td>
<td><code>MEM ← MEM - a (MEM + [2’s complement of a])</code></td>
<td><img src="example-flags" alt="Flags" /></td>
</tr>
<tr>
<td><strong>subc a, M</strong></td>
<td>Subtraction data in memory and carry from ACC, then put result into ACC</td>
<td><code>subc a, MEM;</code></td>
<td><code>a ← a - MEM - C</code></td>
<td><img src="example-flags" alt="Flags" /></td>
</tr>
</tbody>
</table>
**7.3. Shift Operation Instructions**

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Description</th>
<th>Example</th>
<th>Result</th>
<th>Affected Flags</th>
</tr>
</thead>
<tbody>
<tr>
<td>subc M, a</td>
<td>Subtraction ACC and carry bit from memory, then put result into memory</td>
<td><code>subc MEM, a</code></td>
<td><code>MEM ← MEM - a - C</code></td>
<td><code>Y Y Y Y Y Y</code></td>
</tr>
<tr>
<td>subc a</td>
<td>Subtraction carry from ACC, then put result into ACC</td>
<td><code>subc a</code></td>
<td><code>a ← a - C</code></td>
<td><code>Y Y Y Y Y Y</code></td>
</tr>
<tr>
<td>subc M</td>
<td>Subtraction carry from the content of memory, then put result into memory</td>
<td><code>subc MEM</code></td>
<td><code>MEM ← MEM - C</code></td>
<td><code>Y Y Y Y Y Y</code></td>
</tr>
<tr>
<td>inc M</td>
<td>Increment the content of memory</td>
<td><code>inc MEM</code></td>
<td><code>MEM ← MEM + 1</code></td>
<td><code>Y Y Y Y Y Y</code></td>
</tr>
<tr>
<td>dec M</td>
<td>Decrement the content of memory</td>
<td><code>dec MEM</code></td>
<td><code>MEM ← MEM - 1</code></td>
<td><code>Y Y Y Y Y Y</code></td>
</tr>
<tr>
<td>clear M</td>
<td>Clear the content of memory</td>
<td><code>clear MEM</code></td>
<td><code>MEM ← 0</code></td>
<td><code>N N N N N N</code></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Description</th>
<th>Example</th>
<th>Result</th>
<th>Affected Flags</th>
</tr>
</thead>
<tbody>
<tr>
<td>sr a</td>
<td>Shift right of ACC, shift 0 to bit 7</td>
<td><code>sr a</code></td>
<td><code>a (0,b7,b6,b5,b4,b3,b2,b1,0) ← a (b7,b6,b5,b4,b3,b2,b1,b0), C ← a(b0)</code></td>
<td><code>N Y Y Y Y Y</code></td>
</tr>
<tr>
<td>src a</td>
<td>Shift right of ACC with carry bit 7 to flag</td>
<td><code>src a</code></td>
<td><code>a (c,b7,b6,b5,b4,b3,b2,b1) ← a (b7,b6,b5,b4,b3,b2,b1,b0), C ← a(b0)</code></td>
<td><code>N Y Y Y Y Y</code></td>
</tr>
<tr>
<td>sr M</td>
<td>Shift right of the content of memory, shift 0 to bit 7</td>
<td><code>sr MEM</code></td>
<td><code>MEM(0,b7,b6,b5,b4,b3,b2,b1,0) ← MEM(b7,b6,b5,b4,b3,b2,b1,b0), C ← MEM(b0)</code></td>
<td><code>N Y Y Y Y Y</code></td>
</tr>
<tr>
<td>src M</td>
<td>Shift right of memory with carry bit 7 to flag</td>
<td><code>src MEM</code></td>
<td><code>MEM(c,b7,b6,b5,b4,b3,b2,b1) ← MEM (b7,b6,b5,b4,b3,b2,b1,b0), C ← MEM(b0)</code></td>
<td><code>N Y Y Y Y Y</code></td>
</tr>
<tr>
<td>sl a</td>
<td>Shift left of ACC shift 0 to bit 0</td>
<td><code>sl a</code></td>
<td><code>a (b6,b5,b4,b3,b2,b1,b0,0) ← a (b7,b6,b5,b4,b3,b2,b1,b0), C ← a(b7)</code></td>
<td><code>N Y Y Y Y Y</code></td>
</tr>
</tbody>
</table>
slc a  Shift left of ACC with carry bit 0 to flag
Example:           slc  a ;
Result: (b6,b5,b4,b3,b2,b1,b0) ← (b7,b6,b5,b4,b3,b2,b1,b0), C ← a(b7)
Affected flags: 『N』『Y』C 『N』AC 『N』OV

sl M  Shift left of memory, shift 0 to bit 0
Example:           sl M ;
Result: MEM(b6,b5,b4,b3,b2,b1,b0) ← MEM(b7,b6,b5,b4,b3,b2,b1,b0), C ← MEM(b7)
Affected flags: 『N』『Y』C 『N』AC 『N』OV

slc M  Shift left of memory with carry bit 0 to flag
Example:           slc MEM ;
Result: MEM(b6,b5,b4,b3,b2,b1,b0,C) ← MEM(b7,b6,b5,b4,b3,b2,b1,b0), C ← MEM(b7)
Affected flags: 『N』『Y』C 『N』AC 『N』OV

swap a  Swap the high nibble and low nibble of ACC
Example:           swap a ;
Result: a(b3,b2,b1,b0,b7,b6,b5,b4) ← a(b7,b6,b5,b4,b3,b2,b1,b0)
Affected flags: 『N』『Y』C 『N』AC 『N』OV

7.4. Logic Operation Instructions

and a, I  Perform logic AND on ACC and immediate data, then put result into ACC
Example:           and a, 0x0f ;
Result: a ← a & 0fh
Affected flags: 『Y』C 『N』AC 『N』OV

and a, M  Perform logic AND on ACC and memory, then put result into ACC
Example:           and a, RAM10 ;
Result: a ← a & RAM10
Affected flags: 『Y』C 『N』AC 『N』OV

and M, a  Perform logic AND on ACC and memory, then put result into memory
Example:           and MEM, a ;
Result: MEM ← a & MEM
Affected flags: 『Y』C 『N』AC 『N』OV

or a, I  Perform logic OR on ACC and immediate data, then put result into ACC
Example:           or a, 0x0f ;
Result: a ← a | 0fh
Affected flags: 『Y』C 『N』AC 『N』OV

or a, M  Perform logic OR on ACC and memory, then put result into ACC
Example:           or a, MEM ;
Result: a ← a | MEM
Affected flags: 『Y』C 『N』AC 『N』OV

or M, a  Perform logic OR on ACC and memory, then put result into memory
Example:           or MEM, a ;
Result: MEM ← a | MEM
Affected flags: 『Y』C 『N』AC 『N』OV

xor a, I  Perform logic XOR on ACC and immediate data, then put result into ACC
Example:           xor a, 0x0f ;
Result: a ← a ^ 0fh
Affected flags: 『Y』C 『N』AC 『N』OV
<table>
<thead>
<tr>
<th>Operator</th>
<th>Description</th>
<th>Example</th>
<th>Result</th>
<th>Affected Flags</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>xor</code> IO, a</td>
<td>Perform logic XOR on ACC and IO register, then put result into IO register</td>
<td>( \text{xor } pa, a ; )</td>
<td>( pa \leftarrow a ^\wedge \text{pa} ; ) // <code>pa</code> is the data register of port A</td>
<td><code>[N]</code>, <code>[Z]</code>, <code>[N]</code>, <code>[N]</code>, <code>[AC]</code>, <code>[OV]</code></td>
</tr>
<tr>
<td><code>xor</code> a, M</td>
<td>Perform logic XOR on ACC and memory, then put result into ACC</td>
<td><code>xor</code> a, MEM ;</td>
<td>( a \leftarrow a ^\wedge \text{RAM10} )</td>
<td><code>[Y]</code>, <code>[Z]</code>, <code>[N]</code>, <code>[N]</code>, <code>[AC]</code>, <code>[OV]</code></td>
</tr>
<tr>
<td><code>xor</code> M, a</td>
<td>Perform logic XOR on ACC and memory, then put result into memory</td>
<td><code>xor</code> MEM, a ;</td>
<td>( \text{MEM} \leftarrow a ^\wedge \text{MEM} )</td>
<td><code>[Y]</code>, <code>[Z]</code>, <code>[N]</code>, <code>[N]</code>, <code>[AC]</code>, <code>[OV]</code></td>
</tr>
<tr>
<td><code>not</code> a</td>
<td>Perform 1's complement (logical complement) of ACC</td>
<td><code>not</code> a ;</td>
<td>( a \leftarrow \sim a )</td>
<td><code>[Y]</code>, <code>[Z]</code>, <code>[N]</code>, <code>[N]</code>, <code>[AC]</code>, <code>[OV]</code></td>
</tr>
<tr>
<td><code>not</code> M</td>
<td>Perform 1's complement (logical complement) of memory</td>
<td><code>not</code> MEM ;</td>
<td>( \text{MEM} \leftarrow \sim \text{MEM} )</td>
<td><code>[Y]</code>, <code>[Z]</code>, <code>[N]</code>, <code>[N]</code>, <code>[AC]</code>, <code>[OV]</code></td>
</tr>
<tr>
<td><code>neg</code> a</td>
<td>Perform 2's complement of ACC</td>
<td><code>neg</code> a ;</td>
<td>( a \leftarrow \overline{a} )</td>
<td><code>[Y]</code>, <code>[Z]</code>, <code>[N]</code>, <code>[N]</code>, <code>[AC]</code>, <code>[OV]</code></td>
</tr>
</tbody>
</table>

**Application Example:**

```
mov a, 0x38 ; // ACC=0X38
not a ; // ACC=0XC7
```

```
mov a, 0x38 ;
mov mem, a ; // mem = 0x38
not mem ; // mem = 0xC7
```

```
mov a, 0x38 ; // ACC=0X38
neg a ; // ACC=0XC8
```
neg M  Perform 2's complement of memory  
Example:  \textit{neg MEM;}  
Result:  \textit{MEM ← \overline{MEM}}  
Affected flags:  \( \text{Y, Z, N, C, AC, OV} \)  

Application Example:  
\begin{verbatim}  
mov a, 0x38;  
mov mem, a;  // mem = 0x38  
not mem;  // mem = 0xC8  
\end{verbatim}  

7.5. Bit Operation Instructions

\begin{itemize}  
\item \textit{set0} \textit{IO.n}  
Set bit \( n \) of IO port to low  
Example:  \( \textit{set0 pa.5} \)  
Result: set bit 5 of port A to low  
Affected flags:  \( \text{N, Z, C, N, C, AC, N, OV} \)  
\item \textit{set1} \textit{IO.n}  
Set bit \( n \) of IO port to high  
Example:  \( \textit{set1 pa.5} \)  
Result: set bit 5 of port A to high  
Affected flags:  \( \text{N, Z, C, N, C, AC, N, OV} \)  
\item \textit{set0} \textit{M.n}  
Set bit \( n \) of memory to low  
Example:  \( \textit{set0 MEM.5} \)  
Result: set bit 5 of MEM to low  
Affected flags:  \( \text{N, Z, C, N, C, AC, N, OV} \)  
\item \textit{set1} \textit{M.n}  
Set bit \( n \) of memory to high  
Example:  \( \textit{set1 MEM.5} \)  
Result: set bit 5 of MEM to high  
Affected flags:  \( \text{N, Z, C, N, C, AC, N, OV} \)  
\end{itemize}

7.6. Conditional Operation Instructions

\begin{itemize}  
\item \textit{ceqsn} a, l  
Compare ACC with immediate data and skip next instruction if both are equal.  
Flag will be changed like as \( a \leftarrow a \cdot l \)  
Example:  \( \textit{ceqsn a, 0x55; inc MEM; goto error;} \)  
Result: If \( a=0x55 \), then “goto error”; otherwise, “inc MEM”.  
Affected flags:  \( \text{Y, N, Y, Y, Y, AC, Y, OV} \)  
\item \textit{ceqsn} a, M  
Compare ACC with memory and skip next instruction if both are equal.  
Flag will be changed like as \( a \leftarrow a \cdot M \)  
Example:  \( \textit{ceqsn a, MEM;} \)  
Result: If \( a=\text{MEM} \), skip next instruction  
Affected flags:  \( \text{Y, N, Y, Y, Y, AC, Y, OV} \)  
\item \textit{t0sn} IO.n  
Check IO bit and skip next instruction if it’s low  
Example:  \( \textit{t0sn pa.5;} \)  
Result: If bit 5 of port A is low, skip next instruction  
Affected flags:  \( \text{N, Z, N, C, N, AC, N, OV} \)  
\end{itemize}
### 7.7. System control Instructions

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Description</th>
<th>Example</th>
<th>Result</th>
<th>Affected Flags</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>t1sn I.n</strong></td>
<td>Check IO bit and skip next instruction if it's high</td>
<td><code>t1sn pa.5</code></td>
<td>If bit 5 of port A is high, skip next instruction</td>
<td>N, N, N, AC, OV</td>
</tr>
<tr>
<td><strong>t0sn M.n</strong></td>
<td>Check memory bit and skip next instruction if it's low</td>
<td><code>t0sn MEM.5</code></td>
<td>If bit 5 of MEM is low, then skip next instruction</td>
<td>N, N, N, AC, OV</td>
</tr>
<tr>
<td><strong>t1sn M.n</strong></td>
<td>Check memory bit and skip next instruction if it's high</td>
<td>Ex: <code>t1sn MEM.5</code></td>
<td>If bit 5 of MEM is high, then skip next instruction</td>
<td>N, N, N, AC, OV</td>
</tr>
<tr>
<td><strong>izsn a</strong></td>
<td>Increment ACC and skip next instruction if ACC is zero</td>
<td><code>izsn a</code></td>
<td>a ← a + 1, skip next instruction if a = 0</td>
<td>Y, Y, Y, Y, Y</td>
</tr>
<tr>
<td><strong>dzsn a</strong></td>
<td>Decrement ACC and skip next instruction if ACC is zero</td>
<td><code>dzsn a</code></td>
<td>A ← A - 1, skip next instruction if a = 0</td>
<td>Y, Y, Y, Y, Y</td>
</tr>
<tr>
<td><strong>izsn M</strong></td>
<td>Increment memory and skip next instruction if memory is zero</td>
<td><code>izsn MEM</code></td>
<td>MEM ← MEM + 1, skip next instruction if MEM = 0</td>
<td>Y, Y, Y, Y, Y</td>
</tr>
<tr>
<td><strong>dzsn M</strong></td>
<td>Decrement memory and skip next instruction if memory is zero</td>
<td><code>dzsn MEM</code></td>
<td>MEM ← MEM - 1, skip next instruction if MEM = 0</td>
<td>Y, Y, Y, Y, Y</td>
</tr>
</tbody>
</table>

**call label**: Function call, address can be full range address space
Example: `call function1`;
Result: [sp] ← pc + 1
pc ← function1
sp ← sp + 2
Affected flags: N, N, N, AC, OV

**goto label**: Go to specific address which can be full range address space
Example: `goto error`;
Result: Go to error and execute program.
Affected flags: N, N, N, AC, OV

**ret I**: Place immediate data to ACC, then return
Example: `ret 0x55`;
Result: A ← 55h
ret ;
Affected flags: N, N, N, AC, OV
### ret
Return to program which had function call

**Example:** `ret;`

**Result:**
- `sp ← sp - 2`
- `pc ← [sp]`

**Affected flags:**
- N
- Z
- C
- AC
- OV

### reti
Return to program that is interrupt service routine. After this command is executed, global interrupt is enabled automatically.

**Example:** `reti;`

**Affected flags:**
- N
- Z
- C
- AC
- OV

### nop
No operation

**Example:** `nop;`

**Result:** nothing changed

**Affected flags:**
- N
- Z
- C
- AC
- OV

### pcadd a
Next program counter is current program counter plus ACC.

**Example:** `pcadd a;`

**Result:**
- `pc ← pc + a`

**Affected flags:**
- N
- Z
- C
- AC
- OV

**Application Example:**

```assembly
...  mov  a, 0x02;  
      pcadd a;       // PC ← PC+2  
      goto  err1;    
      goto  correct; // jump here  
      goto  err2;    
      goto  err3;    
...  
      correct:       // jump here  
...```

### engint
Enable global interrupt enable

**Example:** `engint;`

**Result:**
- Interrupt request can be sent to FPP0

**Affected flags:**
- N
- Z
- C
- AC
- OV

### disgint
Disable global interrupt enable

**Example:** `disgint;`

**Result:**
- Interrupt request is blocked from FPP0

**Affected flags:**
- N
- Z
- C
- AC
- OV

### stopsys
System halt.

**Example:** `stopsys;`

**Result:**
- Stop the system clocks and halt the system

**Affected flags:**
- N
- Z
- C
- AC
- OV

### stopexe
CPU halt. The oscillator module is still active to output clock, however, system clock is disabled to save power.

**Example:** `stopexe;`

**Result:**
- Stop the system clocks and keep oscillator modules active.

**Affected flags:**
- N
- Z
- C
- AC
- OV
reset | Reset the whole chip, its operation will be same as hardware reset.  
Example: reset;  
Result: Reset the whole chip.  
Affected flags: \(N, Z, N, C, N, AC, N, OV\)

wdreset | Reset Watchdog timer.  
Example: wdreset;  
Result: Reset Watchdog timer.  
Affected flags: \(N, Z, N, C, N, AC, N, OV\)

7.8. Summary of Instructions Execution Cycle

| 2T | goto, call, pcadd, ret, reti, idxm |
| 1T/2T | ceqs1n, cneqs1n, t0sn, t1sn, dzsn, izsn |
| 1T | Others |
7.9. Summary of affected flags by Instructions

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Z</th>
<th>C</th>
<th>AC</th>
<th>OV</th>
<th>Instruction</th>
<th>Z</th>
<th>C</th>
<th>AC</th>
<th>OV</th>
<th>Instruction</th>
<th>Z</th>
<th>C</th>
<th>AC</th>
<th>OV</th>
</tr>
</thead>
<tbody>
<tr>
<td>mov a, l</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>mov M, a</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>mov a, M</td>
<td>Y</td>
<td>-</td>
<td>-</td>
<td>-</td>
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<td>Y</td>
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<td>goto label</td>
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<td>reset</td>
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<td>wdreset</td>
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</table>
### 8. Code Options

<table>
<thead>
<tr>
<th>Option</th>
<th>Selection</th>
<th>Description</th>
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<tbody>
<tr>
<td>Security</td>
<td>Enable</td>
<td>Security Enable</td>
</tr>
<tr>
<td></td>
<td>Disable</td>
<td>Security Disable</td>
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<tr>
<td>LVR</td>
<td>4.0V</td>
<td>Select LVR = 4.0V</td>
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<td></td>
<td>3.5V</td>
<td>Select LVR = 3.5V</td>
</tr>
<tr>
<td></td>
<td>3.0V</td>
<td>Select LVR = 3.0V</td>
</tr>
<tr>
<td></td>
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<td>Select LVR = 2.75V</td>
</tr>
<tr>
<td></td>
<td>2.5V</td>
<td>Select LVR = 2.5V</td>
</tr>
<tr>
<td></td>
<td>2.2V</td>
<td>Select LVR = 2.2V</td>
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<tr>
<td></td>
<td>2.0V</td>
<td>Select LVR = 2.0V</td>
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<tr>
<td></td>
<td>1.8V</td>
<td>Select LVR = 1.8V</td>
</tr>
<tr>
<td>Boot-up Time</td>
<td>Slow</td>
<td>Please refer to ( t_{WUP} ) and ( t_{SBP} ) in Section 4.1</td>
</tr>
<tr>
<td></td>
<td>Fast</td>
<td>Please refer to ( t_{WUP} ) and ( t_{SBP} ) in Section 4.1</td>
</tr>
<tr>
<td>Drive</td>
<td>Low</td>
<td>IO Low driving and sinking current</td>
</tr>
<tr>
<td></td>
<td>Normal</td>
<td>IO Normal driving and sinking current</td>
</tr>
</tbody>
</table>
9. Special Notes

This chapter is to remind user who use PMS150C series IC in order to avoid frequent errors upon operation.

9.1. Warning

User must read all application notes of the IC by detail before using it. Please download the relative application notes from the following link:


9.2. Using IC

9.2.1. IO pin usage and setting

(1) IO pin as digital input
   ◆ When IO is set as digital input, the level of Vih and Vil would changes with the voltage and temperature. Please follow the minimum value of Vih and the maximum value of Vil.
   ◆ The value of internal pull high resistor would also changes with the voltage, temperature and pin voltage. It is not the fixed value.

(2) If IO pin is set to be digital input and enable wake-up function
   ◆ Configure IO pin as input
   ◆ Set corresponding bit to “1” in PADIER
   ◆ For those IO pins of PA that are not used, PADIER[1:2] should be set low in order to prevent them from leakage.

(3) PA5 is set to be output pin
   ◆ PA5 can be set to be Open-Drain output pin only, output high requires adding pull-up resistor.

(4) PA5 is set to be PRST# input pin
   ◆ Configure PA5 as input
   ◆ Set CLKMD.0=1 to enable PA5 as PRST# input pin

(5) PA5 is set to be input pin and to connect with a push button or a switch by a long wire
   ◆ Needs to put a >10Ω resistor in between PA5 and the long wire
   ◆ Avoid using PA5 as input in such application.

9.2.2. Interrupt

(1) When using the interrupt function, the procedure should be:
   Step1: Set INTEN register, enable the interrupt control bit
   Step2: Clear INTRQ register
   Step3: In the main program, using ENGINT to enable CPU interrupt function
   Step4: Wait for interrupt. When interrupt occurs, enter to Interrupt Service Routine
   Step5: After the Interrupt Service Routine being executed, return to the main program
   * Use DISGINT in the main program to disable all interrupts
* When interrupt service routine starts, use PUSHAF instruction to save ALU and FLAG register. POPAF instruction is to restore ALU and FLAG register before RETI as below:

```c
void Interrupt (void)   // Once the interrupt occurs, jump to interrupt service routine
{
  // enter DISGINT status automatically, no more interrupt is accepted
  PUSHAF;
  ...
  POPAF;
}   // RETI will be added automatically. After RETI being executed, ENGINT status will be restored.
```

(2) INTEN and INTRQ have no initial values. Please set required value before enabling interrupt function.

### 9.2.3. System clock switching

System clock can be switched by CLKMD register. Please notice that, NEVER switch the system clock and turn off the original clock source at the same time. For example: When switching from clock A to clock B, please switch to clock B first; and after that turn off the clock A oscillator through CLKMD.

- **Example:** Switch system clock from ILRC to IHRC/2
  
  ```
  CLKMD  =   0x36;         // switch to IHRC, ILRC can not be disabled here
  CLKMD.2 =   0;        // ILRC can be disabled at this time
  ```

- **ERROR:** Switch ILRC to IHRC and turn off ILRC simultaneously
  
  ```
  CLKMD   =   0x50;       // MCU will hang
  ```

### 9.2.4. Power down mode, wakeup and watchdog

Watchdog will be inactive once ILRC is disabled.

### 9.2.5. TIMER time out

When select T16M counter BIT8 as 1 to generate interrupt, the first interrupt will occur when the counter reaches to 0x100 (BIT8 from 0 to 1) and the second interrupt will occur when the counter reaches 0x300 (BIT8 from 0 to 1). Therefore, selecting BIT8 as 1 to generate interrupt means that the interrupt occurs every 512 counts. Please notice that if T16M counter is restarted, the next interrupt will occur once BIT8 turns from 0 to 1.

### 9.2.6. IHRC

1. The IHRC frequency calibration is performed when IC is programmed by the writer.
2. Because the characteristic of the Epoxy Molding Compound (EMC) would some degrees affects the IHRC frequency (either for package or COB), if the calibration is done before molding process, the actual IHRC frequency after molding may be deviated or becomes out of spec. Normally , the frequency is getting slower a bit.
3. It usually happens in COB package or Quick Turnover Programming (QTP). And PADAUK would not take any responsibility for this situation.
4. Users can make some compensatory adjustments according to their own experiences. For example, users can set IHRC frequency to be 0.5% ~ 1% higher and aim to get better re-targeting after molding.
9.2.7. LVR

(1) V_{DD} must reach or above 2.0V for successful power-on process; otherwise IC will be inactive.
(2) The setting of LVR (1.8V ~ 4.0V) will be valid just after successful power-on process.
(3) User can set MISC.2 as “1” to disable LVR. However, V_{DD} must be kept as exceeding the lowest working voltage of chip; Otherwise IC may work abnormally.

9.2.8. Instructions

(1) There are 79 instructions are provided by PMS150C.
(2) Only single FPPA is built inside the PMS150C, the executing cycles for different instructions are shown as below:

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Condition</th>
<th>CPU</th>
</tr>
</thead>
<tbody>
<tr>
<td>goto, call, pcadd, ret, reti</td>
<td>Condition is fulfilled</td>
<td>2T</td>
</tr>
<tr>
<td>ceqsn, cneqsn, t0sn, t1sn, dzsn, izsn</td>
<td>Condition is not fulfilled</td>
<td>1T</td>
</tr>
<tr>
<td>idxm</td>
<td></td>
<td>2T</td>
</tr>
<tr>
<td>Others</td>
<td></td>
<td>1T</td>
</tr>
</tbody>
</table>

9.2.9. RAM definition

(1) Bit defined: Only addressed at 0x00 ~ 0x0F
(2) WORD defined : Only addressed at 0x00 ~ 0x1E

9.2.10. Program writing

There are 6 pins for using the writer to program: PA3, PA4, PA5, PA6, VDD and GND.

Please use PDK3S-P-002 for program real chip and just use the CN38 jumper (at the back for the writer) with putting the PMS150-S08/DIP8 IC downward three spaces on the Textool. Other packages could be programmed by connecting the signals correspondingly. All the signals of the left side of the jumpers are the same and as the descriptions at the left bottom corner. They are VDD, PA0(not used), PA3, PA4, PA5, PA6, PA7(not used), and GND).

If user use PDK5S-P-003 or above to program, please follow the instructions for connecting jumpers.
9.3. Using ICE

Please use 5S-I-S0xx ICE to emulate most of PMS150C function except as the list below:

(1) 5S-I-S0xx doesn’t support SYSCLK=ILRC/16
(2) 5S-I-S0xx doesn’t support PA6 and PA7 as the CIN2- and CIN3- of the comparator.
(3) 5S-I-S0xx doesn’t support TM2PWM output of PA4.
(4) 5S-I-S0xx doesn’t support the INTEGS the Bit[7:6] dynamically switched.
(5) When GPCS[7]=1, the output of PA0 will affect the High function of PA3.
(6) Fast Wakeup time is different from PDK5S-I-S0xx: 128 SysClk, PMS150C: 32 ILRC
(7) Watch dog time out period is different from PDK5S-I-S0xx:

<table>
<thead>
<tr>
<th>WDT period</th>
<th>PMS150C</th>
<th>PDK5S-I-S0xx</th>
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</thead>
<tbody>
<tr>
<td>misc[1:0]=00</td>
<td>8K* T_{ILRC}</td>
<td>2048* T_{ILRC}</td>
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<tr>
<td>misc[1:0]=01</td>
<td>16K* T_{ILRC}</td>
<td>4096* T_{ILRC}</td>
</tr>
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<td>misc[1:0]=10</td>
<td>64K* T_{ILRC}</td>
<td>16384* T_{ILRC}</td>
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<tr>
<td>misc[1:0]=11</td>
<td>256K* T_{ILRC}</td>
<td>256* T_{ILRC}</td>
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